


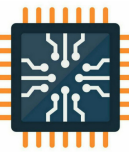
HuaQin Confidential

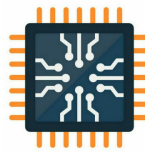
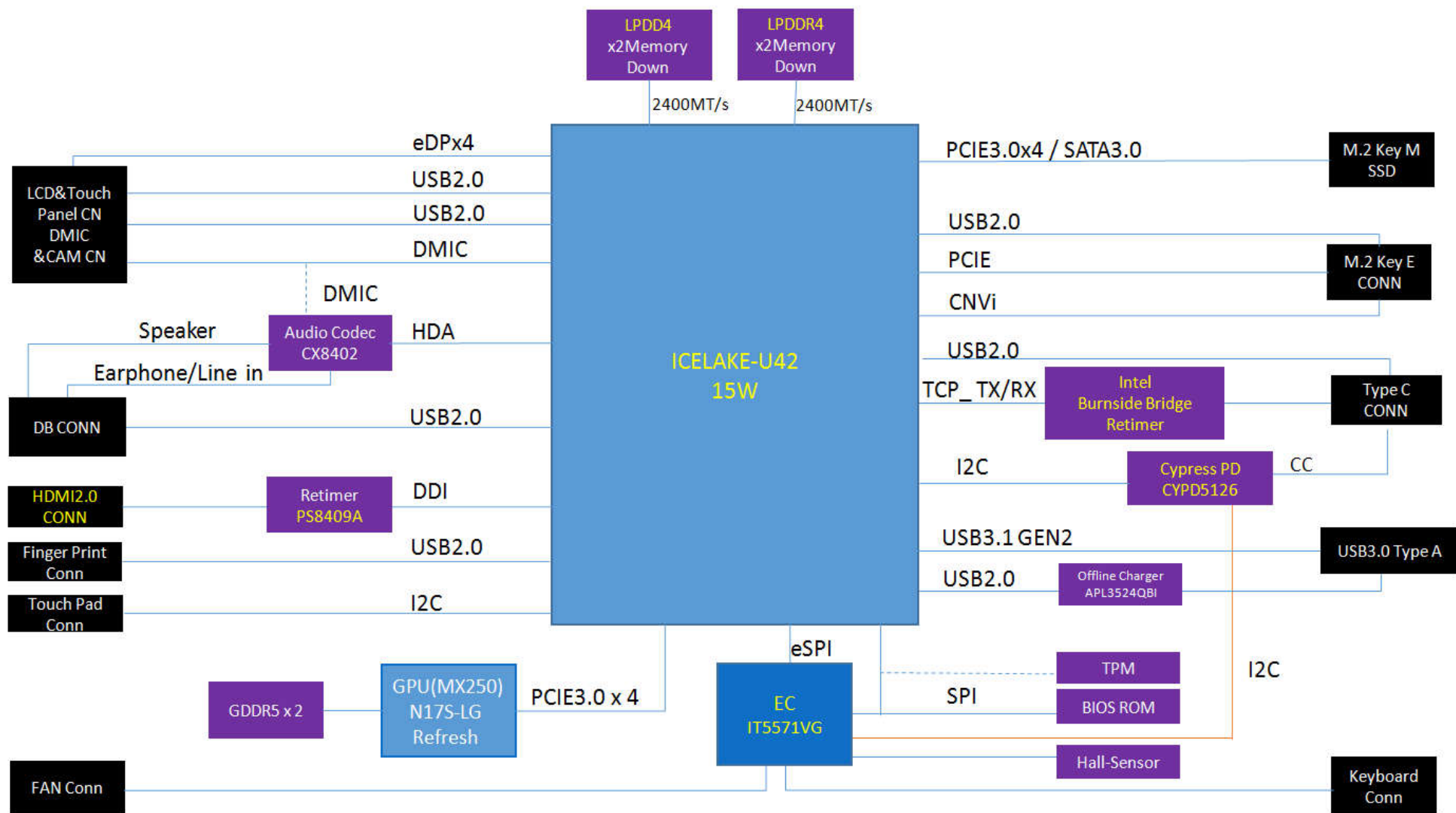
NB8511/12_M/B Schematics Document Intel ICL Lake U-Processor with LPDDR4

REV1.0

2019-02-01

Author	Leo.Liu & Payne.Zhang	 Huaqin Telecom Technology Com.,Ltd.	
Reviewer	Nelosl.Hai & Nemo.Jiang	Page name: Cover page	
Approver	Lobo_Fan	Size: A4 Project Name: NB8511 Date: Monday, July 15, 2019	REV: V1.0 Sheet: 1 of 72





MEM ID

HW_ID3	HW_ID2	HW_ID1	HW_ID0	Description	Total
0	0	0	0	SAMSUNG LPDDR4 3733 1GB K4F8E304HB-MGCJ LF+HF D20	4GB
0	0	0	1	HYNIX LPDDR4 3733 1GB H9HCNNN8KUMLHR-NME LF+HF DDP	4GB
0	0	1	0	MICRON LPDDR4 4266 2GB MT53E512M32D2NP-046 WT:E LF+HF Z11N	8GB
0	1	0	0	HYNIX LPDDR4 3733 2GB H9HCNNNBPUMLHR-NME LF+HF DE	8GB
0	1	0	0		16GB
1	0	0	0	HYNIX LPDDR4X 4266 4GB H9HCNNNCFMALHR-NEE LF+HF QDP	
				4x 16Gb(reserve)	

GPU ID


HW_ID5	HW_ID4	Description	
		N17-LG-Refresh	N17-LG
0	0	NC	NC
1	0	Mount	
1	1		Mount

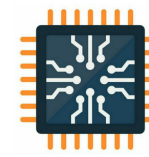
KB BL ID

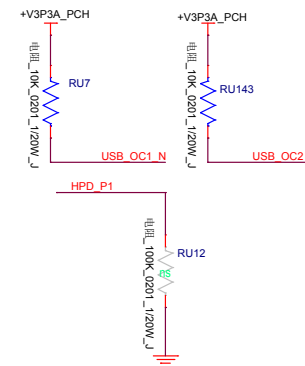
HW_ID6	Description
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1	Keyboard Backlight

Reserve ID

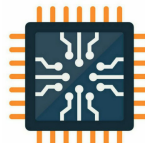
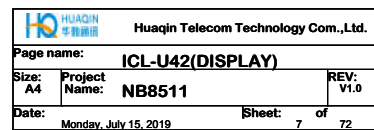
HW_ID7	Description
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1	Reserve

 HUAQIN 华勤通信		Huaqin Telecom Technology Com.,Ltd.	
Page name: I2C Table			
Size: A4	Project Name: NB8511	REV: V1.0	
Date: Monday, July 15, 2019	Sheet: 3		of 72





```
TBT LSx0 RXD
0: DDP1 I2C / TBT LSx #0 / BSSB_LS #0 pins at 1.8V
1: DDP1 I2C / TBT LSx #0 / BSSB_LS #0 pins at 3.3V
```





GPU

29 PCIE_CRX_GTX_N2 >> PCIE CRX GTX N2
29 PCIE_CRX_GTX_P2 >> PCIE CRX GTX P2
29 PCIE_CTX_GRX_N2 >> PCIE CTX GRX N2 C
29 PCIE_CTX_GRX_P2 >> PCIE CTX GRX P2 C

29 PCIE_CRX_GTX_N3 >> PCIE CRX GTX N3
29 PCIE_CRX_GTX_P3 >> PCIE CRX GTX P3
29 PCIE_CTX_GRX_N3 >> PCIE CTX GRX N3 C
29 PCIE_CTX_GRX_P3 >> PCIE CTX GRX P3 C

NA

WLAN

43 PCIE_WLAN_RX_DN >> PCIE WLAN RX DN
43 PCIE_WLAN_RX_DP >> PCIE WLAN RX DP
43 PCIE_WLAN_TX_DN >> PCIE WLAN TX DN
43 PCIE_WLAN_TX_DP >> PCIE WLAN TX DP

SSD1

41 PCIE13_CRX_DTX_N >> PCIE13_CRX_DTX_N
41 PCIE13_CRX_DTX_P >> PCIE13_CRX_DTX_P
41 PCIE13_CTX_DRX_N >> PCIE13_CTX_DRX_N
41 PCIE13_CTX_DRX_P >> PCIE13_CTX_DRX_P

41 PCIE14_CRX_DTX_N >> PCIE14_CRX_DTX_N
41 PCIE14_CRX_DTX_P >> PCIE14_CRX_DTX_P
41 PCIE14_CTX_DRX_N >> PCIE14_CTX_DRX_N
41 PCIE14_CTX_DRX_P >> PCIE14_CTX_DRX_P

41 PCIE15_CRX_DTX_N >> PCIE15_CRX_DTX_N
41 PCIE15_CRX_DTX_P >> PCIE15_CRX_DTX_P
41 PCIE15_CTX_DRX_N >> PCIE15_CTX_DRX_N
41 PCIE15_CTX_DRX_P >> PCIE15_CTX_DRX_P

41 PCIE16_SATA_CRX_DTX_N >> PCIE16_SATA_CRX_DTX_N
41 PCIE16_SATA_CRX_DTX_P >> PCIE16_SATA_CRX_DTX_P
41 PCIE16_SATA_CTX_DRX_N >> PCIE16_SATA_CTX_DRX_N
41 PCIE16_SATA_CTX_DRX_P >> PCIE16_SATA_CTX_DRX_P

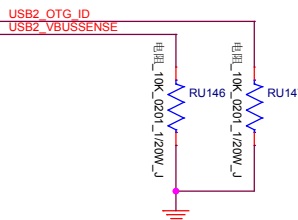
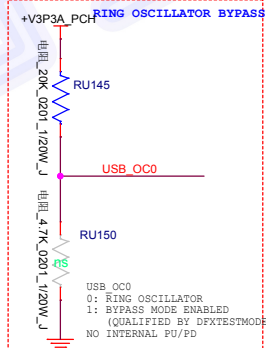
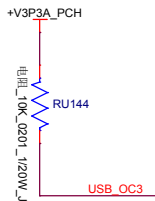
10.41 SSD1_DET >> SSD1_DET

49 USB_OC0 >> USB_OC0
54 USB_OC3 >> USB_OC3

41 SATA1_DEVS LP << SATA1_DEVS LP



PCH STRAP



ICL_U_IP_EXT_WW20

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777

PCIE1_RXN/USB31_1_RXN
PCIE1_RXP/USB31_1_RXP
PCIE1_TXN/USB31_1_TXN
PCIE1_TXP/USB31_1_TXP

PCIE2_RXN/USB31_2_RXN
PCIE2_RXP/USB31_2_RXP
PCIE2_TXN/USB31_2_TXN
PCIE2_TXP/USB31_2_TXP

PCIE3_RXN/USB31_3_RXN
PCIE3_RXP/USB31_3_RXP
PCIE3_TXN/USB31_3_TXN
PCIE3_TXP/USB31_3_TXP

PCIE4_RXN/USB31_4_RXN
PCIE4_RXP/USB31_4_RXP
PCIE4_TXN/USB31_4_TXN
PCIE4_TXP/USB31_4_TXP

PCIE5_RXN/USB31_5_RXN
PCIE5_RXP/USB31_5_RXP
PCIE5_TXN/USB31_5_TXN
PCIE5_TXP/USB31_5_TXP

PCIE6_RXN/USB31_6_RXN
PCIE6_RXP/USB31_6_RXP
PCIE6_TXN/USB31_6_TXN
PCIE6_TXP/USB31_6_TXP

USB2N_1

USB2P_1

USB2N_2

USB2P_2

USB2N_3

USB2P_3

USB2N_4

USB2P_4

USB2N_5

USB2P_5

USB2N_6

USB2P_6

USB2N_7

USB2P_7

USB2N_8

USB2P_8

USB2N_9

USB2P_9

USB2N_10

USB2P_10

USB_ID

USB_VBUSSENSE

USB_COMP

RSVD_BSCAN

7

USB3_P1_RX_DN
USB3_P1_RX_DP
USB3_P1_TX_DN
USB3_P1_TX_DP

USB3_P1_RX_DN
USB3_P1_RX_DP
USB3_P1_TX_DN
USB3_P1_TX_DP

USB3_P1_RX_DN
USB3_P1_RX_DP
USB3_P1_TX_DN
USB3_P1_TX_DP

USB3_P1_RX_DN
USB3_P1_RX_DP
USB3_P1_TX_DN
USB3_P1_TX_DP

USB3_P1_RX_DN
USB3_P1_RX_DP
USB3_P1_TX_DN
USB3_P1_TX_DP

USB3_P1_RX_DN
USB3_P1_RX_DP
USB3_P1_TX_DN
USB3_P1_TX_DP

USB2N_1

USB2P_1

USB2N_2

USB2P_2

USB2N_3

USB2P_3

USB2N_4

USB2P_4

USB2N_5

USB2P_5

USB2N_6

USB2P_6

USB2N_7

USB2P_7

USB2N_8

USB2P_8

USB2N_9

USB2P_9

USB2N_10

USB2P_10

USB_ID

USB_VBUSSENSE

USB_COMP

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

RSVD_BSCAN

USB3.0 TypeA 1 AUO

NA

NA

NA

NA

GPU

USB3.0 Type-A 1 AUO

NA

Type-C

DB USB2.0 Type-A

Finger Print

Camera

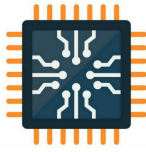
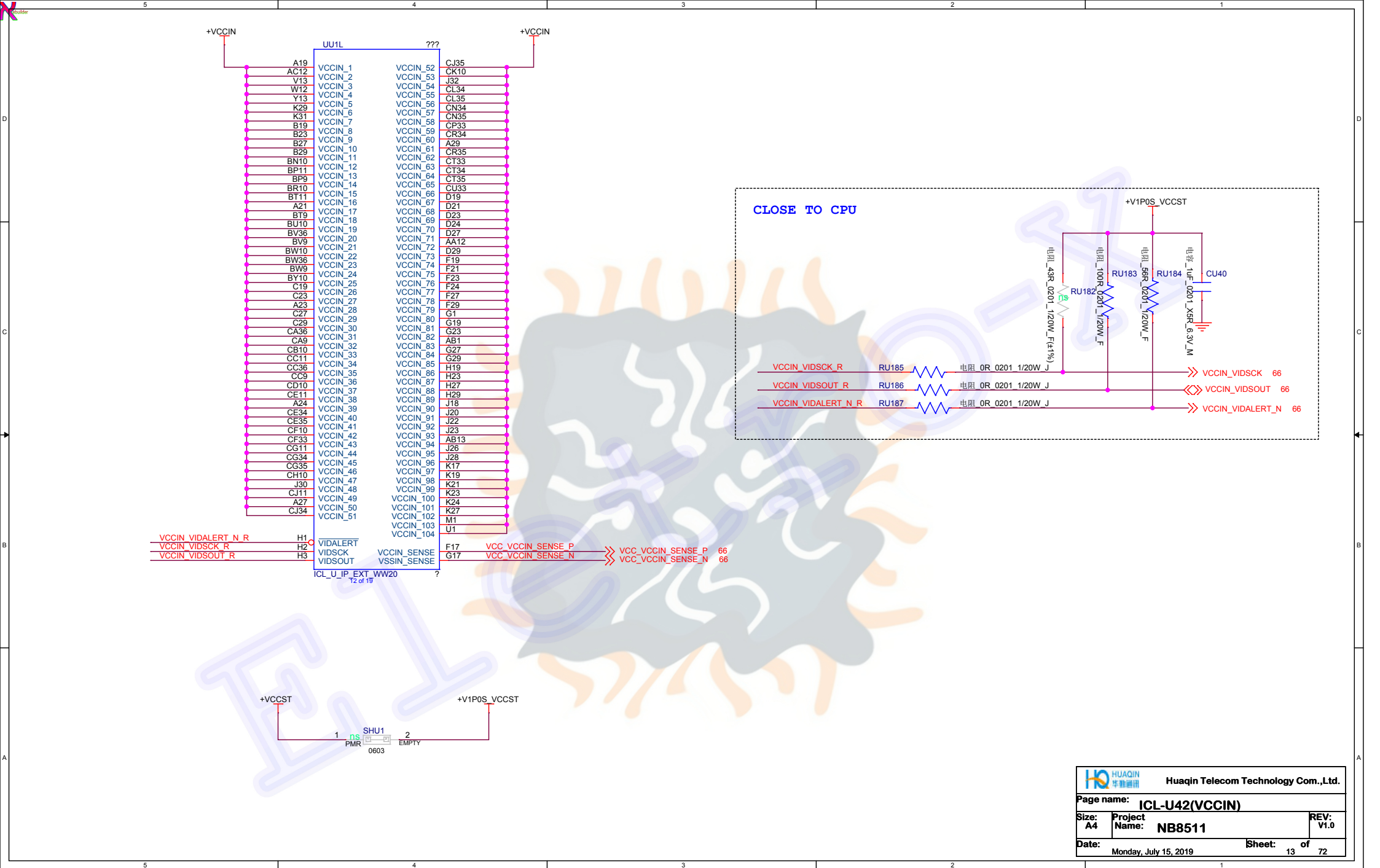
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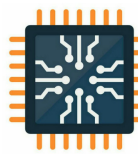
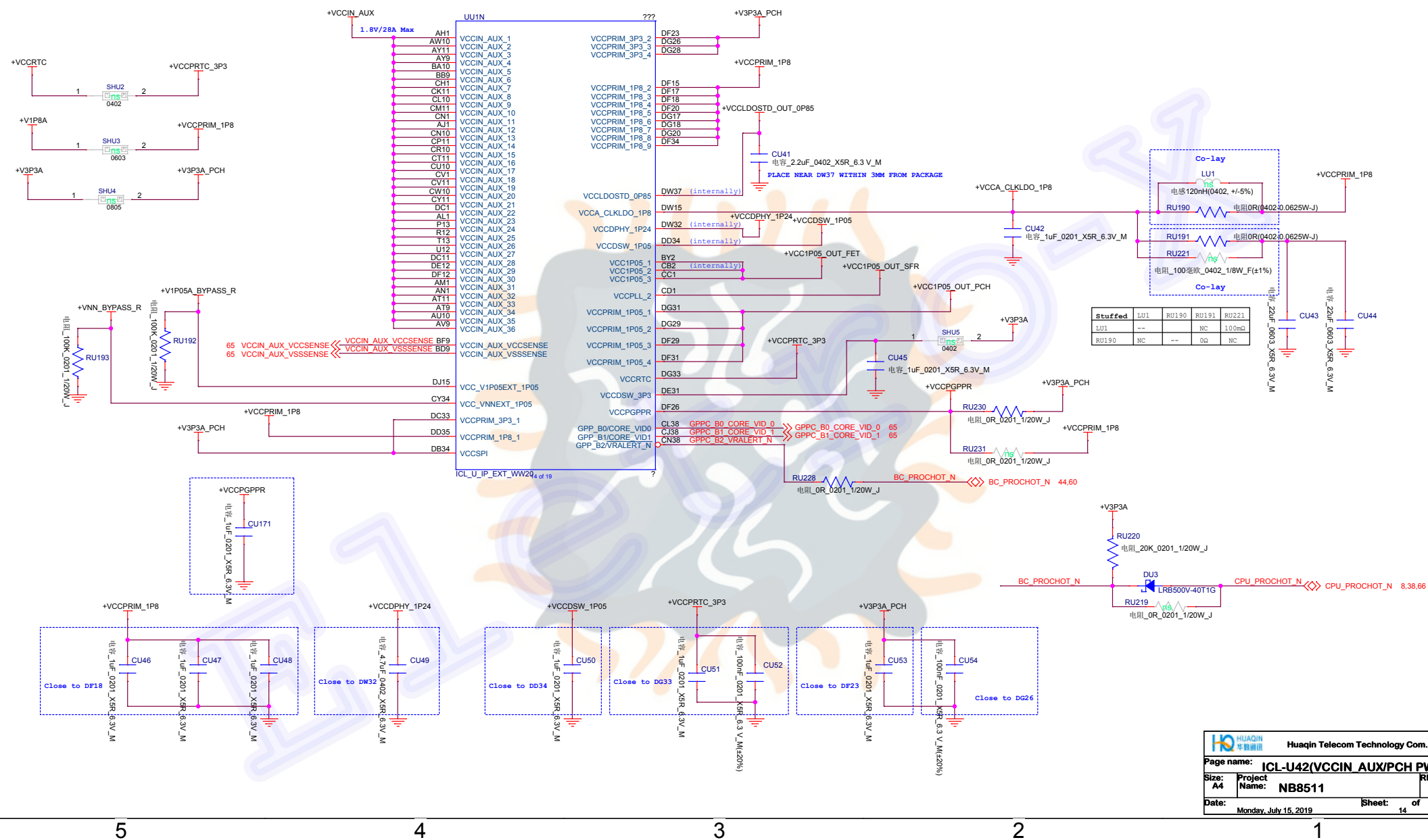
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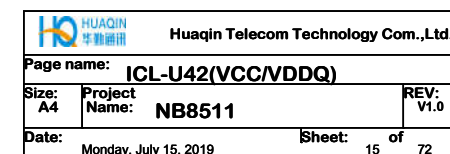
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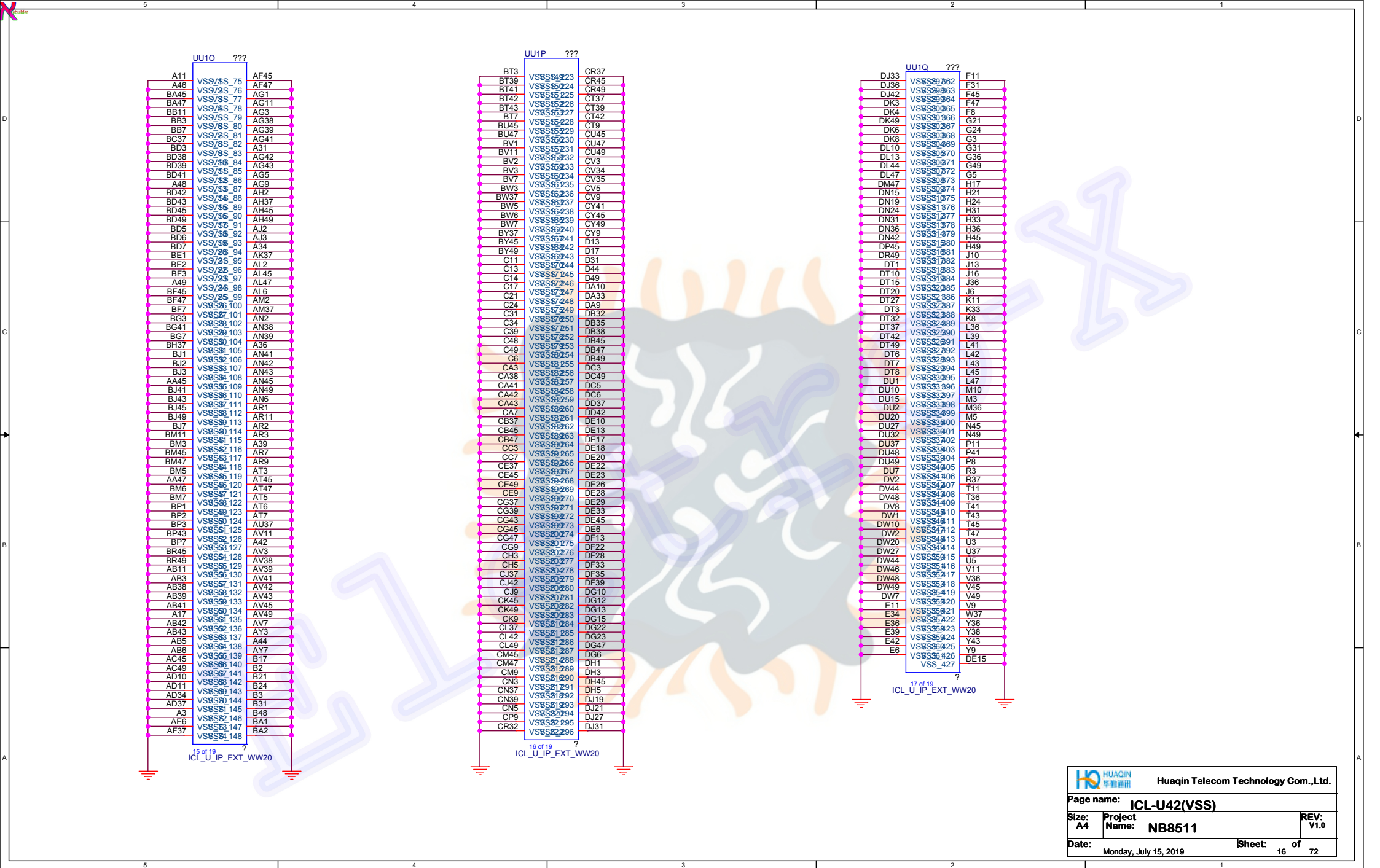
BT

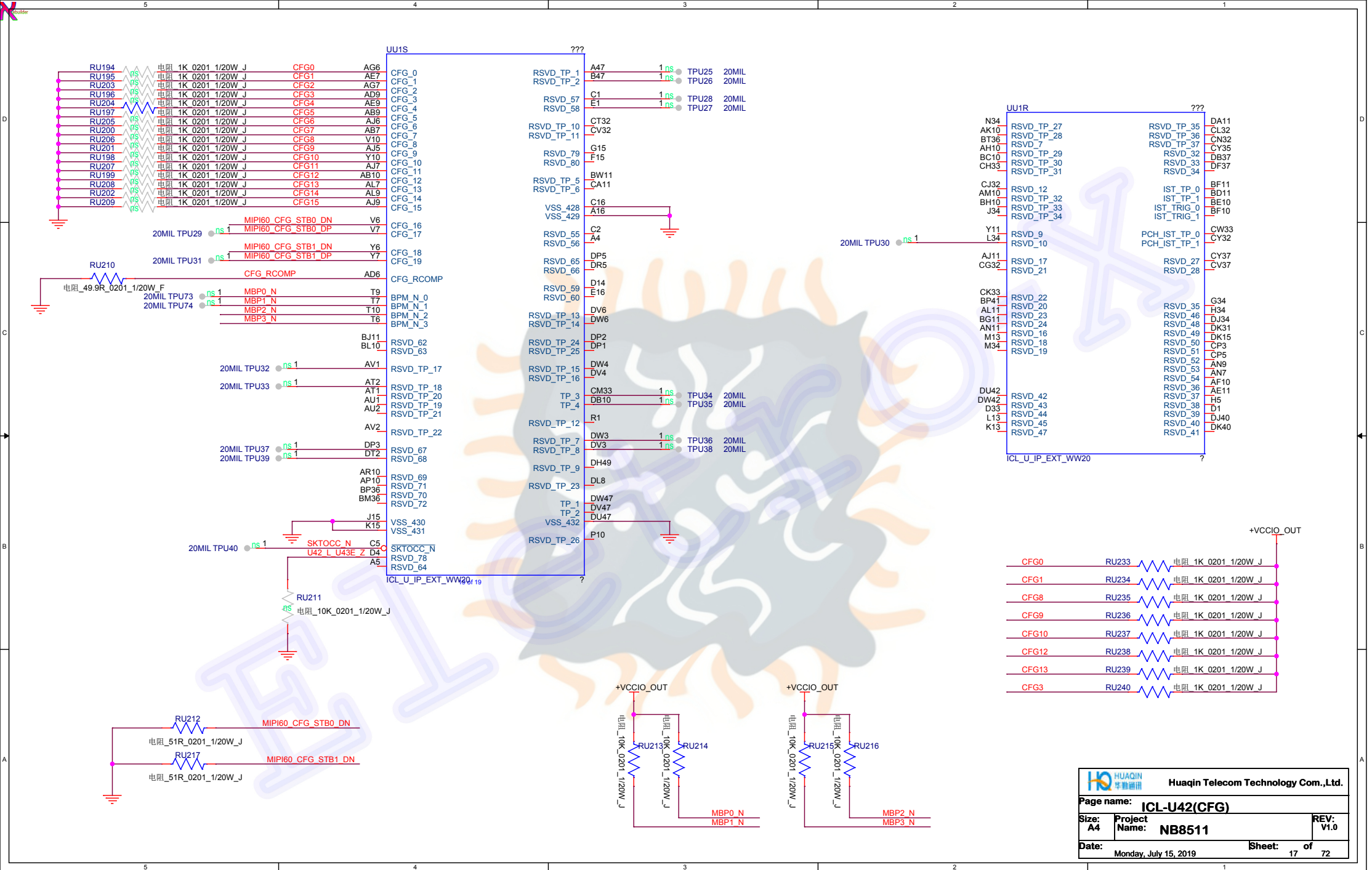
USB2 COMP2 RESISTOR SHOULD
BE PLACED NEAR TO THE PIN
LENGHT <450 MILS

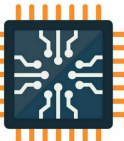




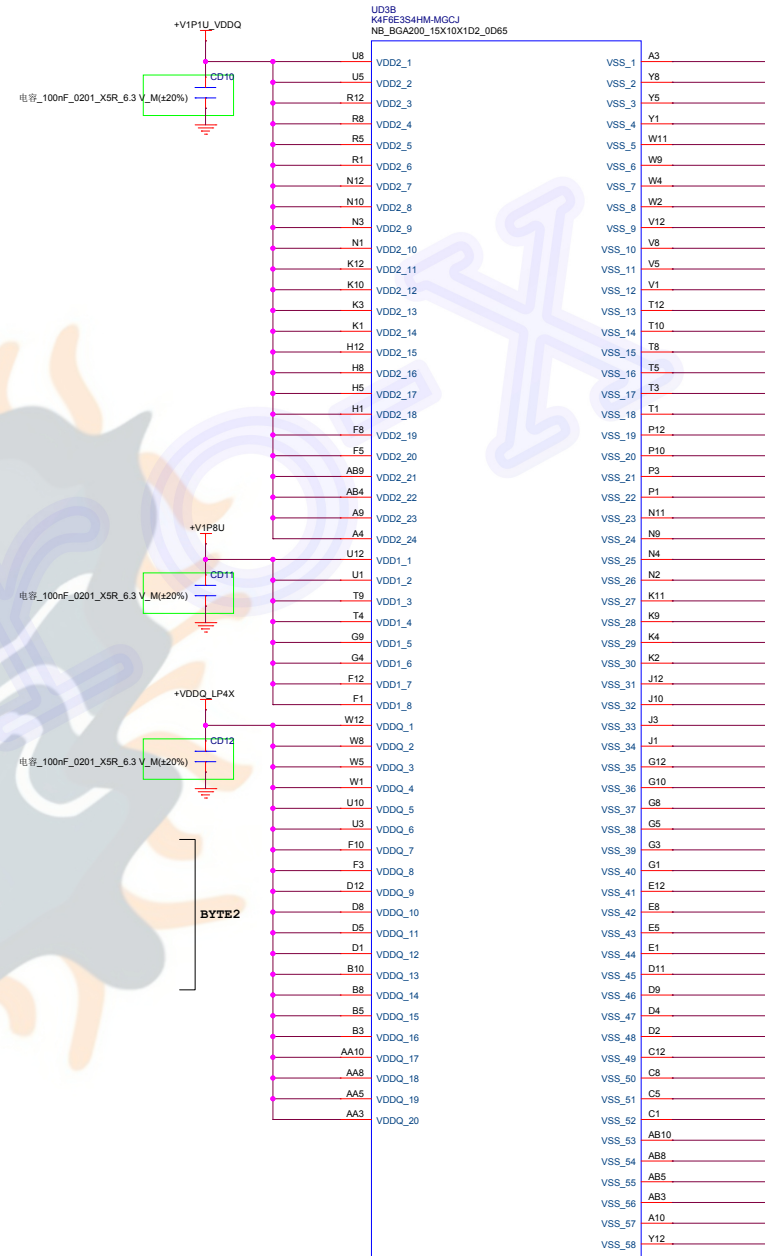


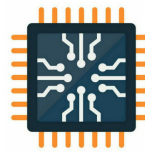
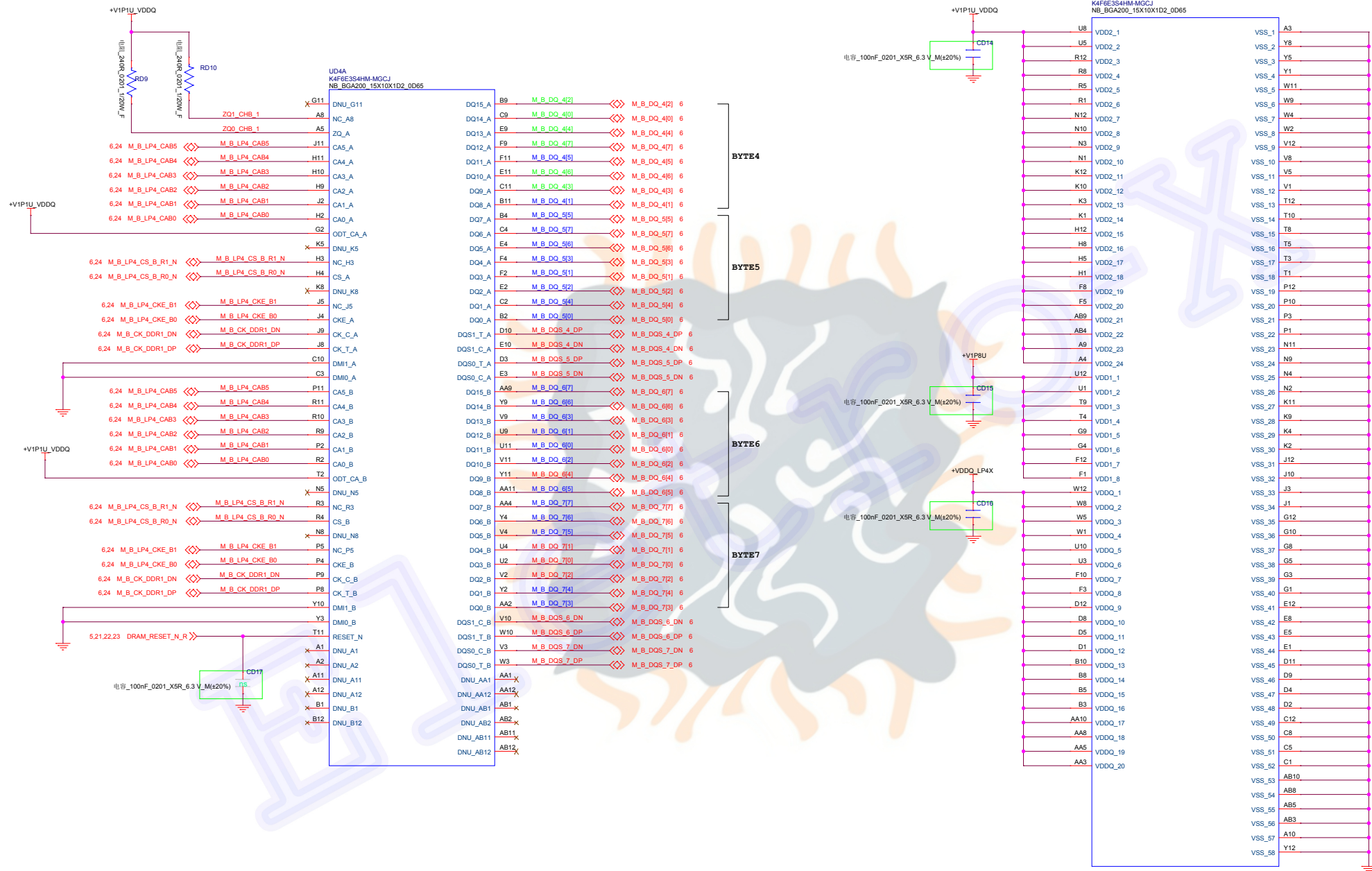


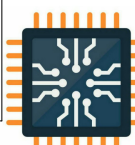
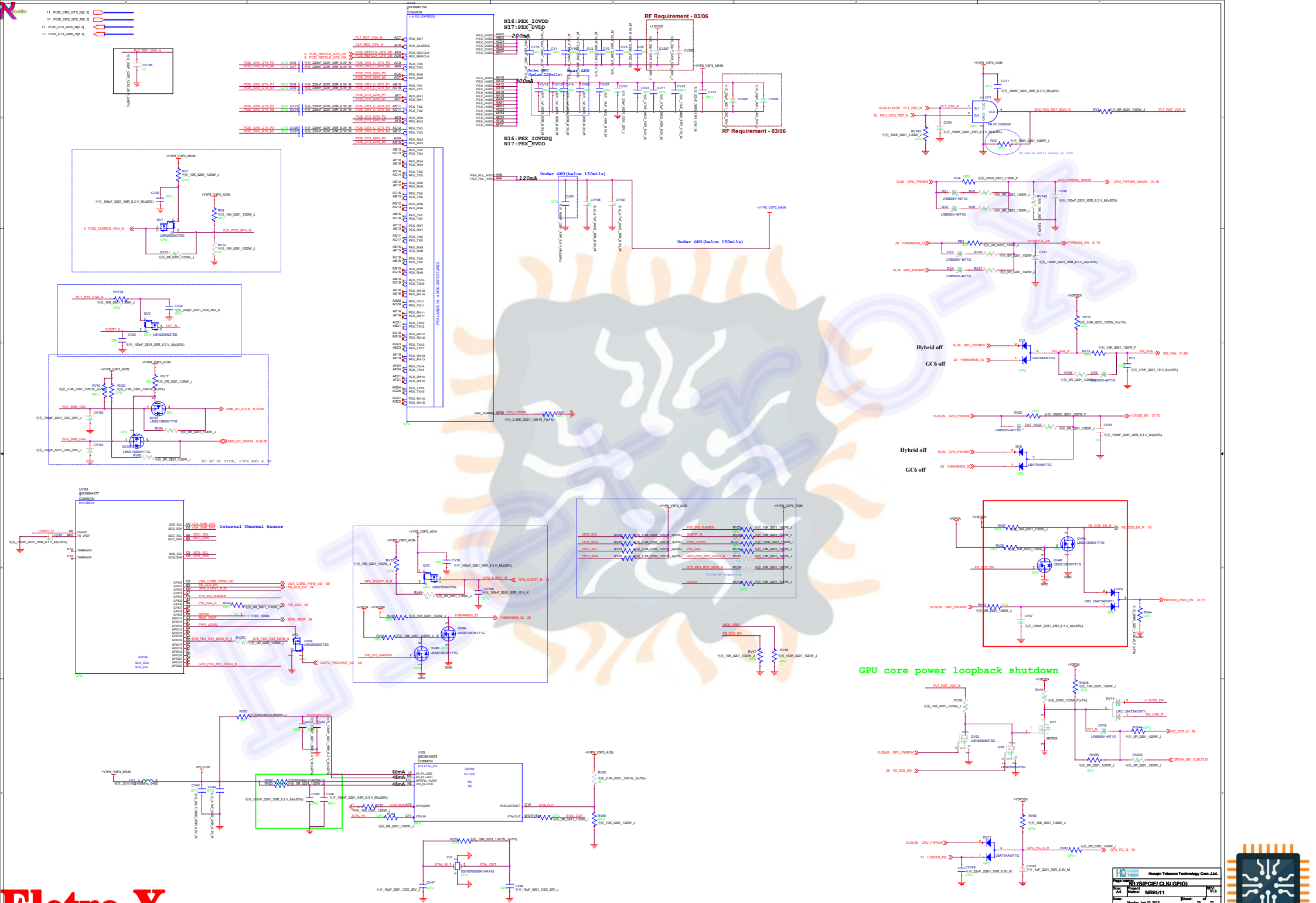


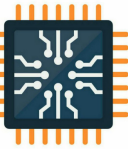
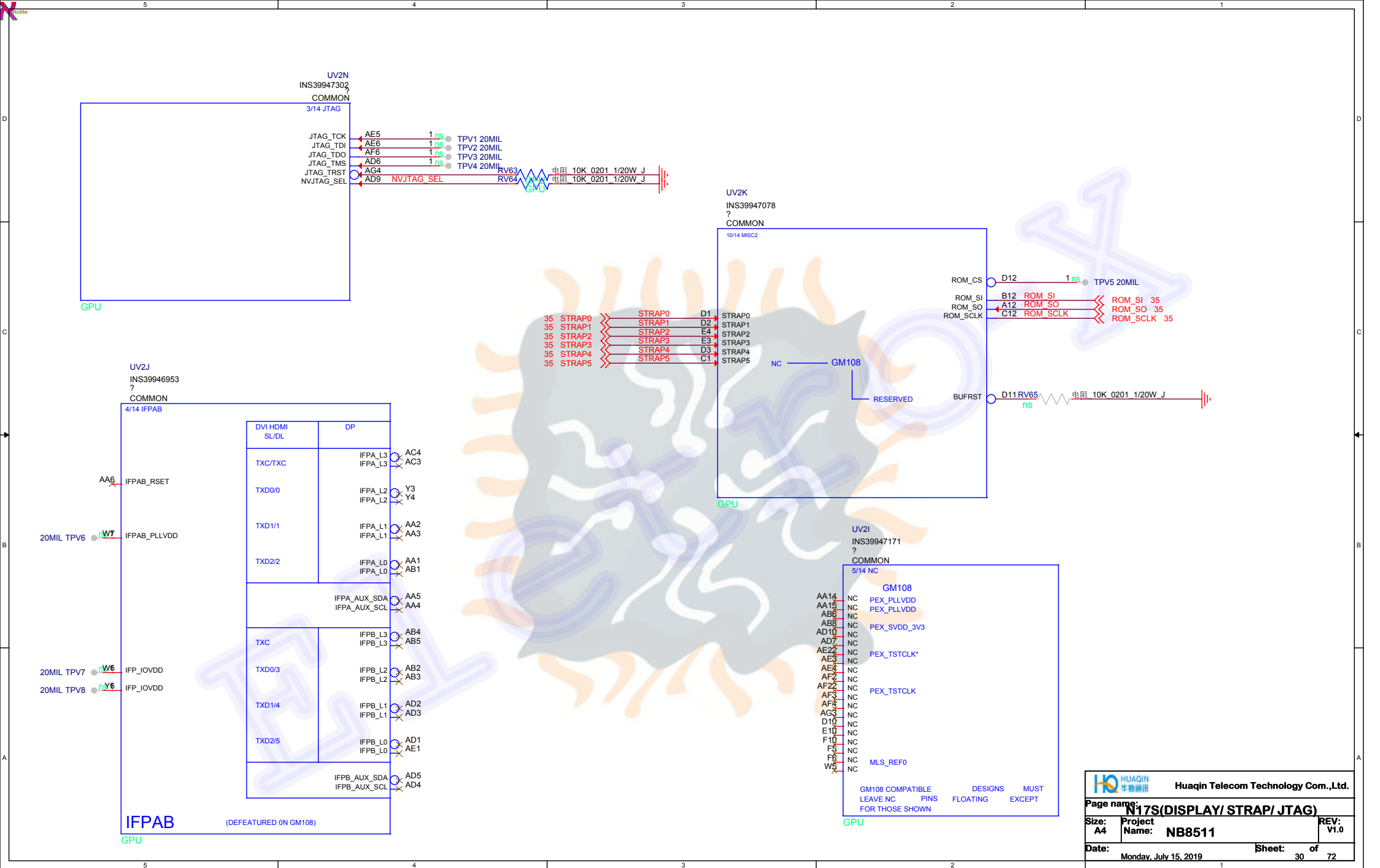


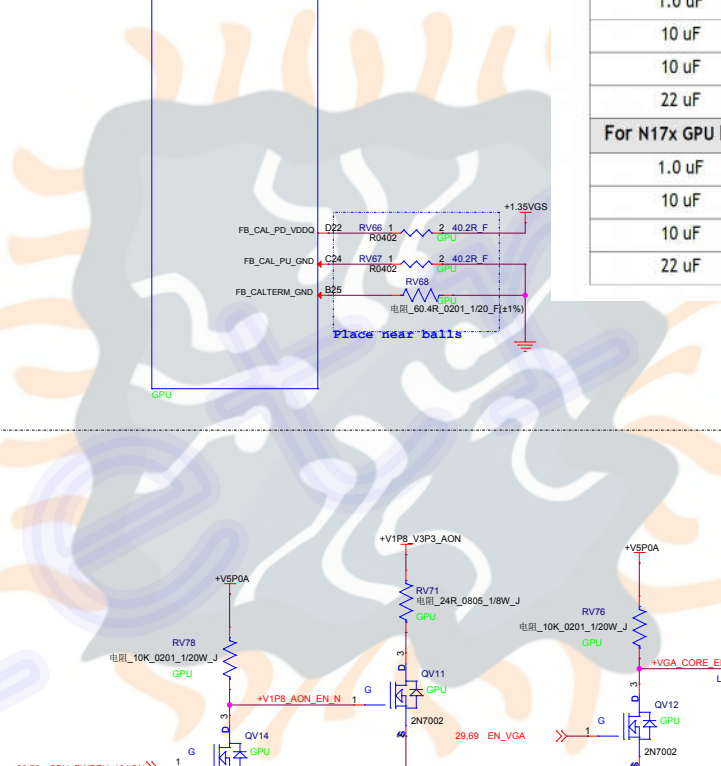












FBVDDQ Decoupling Requirements		
	Recommended Quantity and Placement (for all supported partitions combined)	
Size	Quantity	Placement
2C-64 (preliminary)		
6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
6S [0603]	2	
6S [0603]	1	Near GPU device
6S [0603]	3	
4C-128 (preliminary)		
6S [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	4	
6S [0603]	2	Near GPU device
6S [0603]	5	
B4-256		
6S [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	5	
6S [0603]	7	Near GPU device
6S [0603]	9	

FBVDDQ Decoupling Requirements		
	Recommended Quantity and Placement (for all supported partitions combined)	
Size	Quantity	Placement
2C-64 (preliminary)		
6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
6S [0603]	2	
6S [0603]	1	Near GPU device
6S [0603]	3	
4C-128 (preliminary)		
6S [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	4	
6S [0603]	2	Near GPU device
6S [0603]	5	
B4-256		
6S [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	5	
6S [0603]	7	Near GPU device
6S [0603]	9	

Move to Power Page 2018/06/07

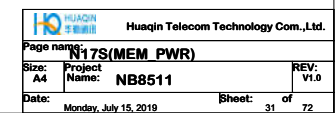


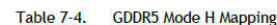
Table 7.18 GB2C-64 Package: Power Rail Filtering


Rail (GPU Ball) Name	Balls	Voltage: Current	Filtering under GPU	Filtering Near GPU
NVVDD	31	Varies	3 X 1uF (0402) 8 X 4.7uF (0603)	4 X 4.7uF (0805) 4 X 10uF (0805) 3 X 22uF (0805) 1 X 330uF (Pocscap) Near VR: 2 X 10uF (0805)
NVVDD_S	10	Varies	2 X 1uF (0402) 4 X 4.7uF (0603)	7 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Pocscap)
FBVDDQ (GPU side) ¹	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 300 bead (0603 max< ESR 10 mΩ)
FBB_PLL_AVDD	1	1.8V	0.1uF (0402 X5R)	1 X 22uF (0805)
FB_REFPLL_AVDD	1	1.8V	1 X 0.1uF (0402 X5R)	
IFPAB_PLLVDD	1	1.8V	2 X 0.1uF (0402 X5R)	1 X 300 bead (0603 max< ESR 0.01 Ω)
GPCPLL_AVDD	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 4.7uF (0602)
XS_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	
SP_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	
WD_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	
IFP_OVDD	2	1.0V	2 X 0.1uF (0402 X6S)	1 X 4.7uF (0603) 1 X 1uF (0402)

Table 7.18 GB2C-64 Package: Power Rail Filtering (Continued)

Rail (GPU Ball) Name	Balls	Voltage: Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
1VB_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402)
1VB_AON	2	1.8V	2 X 0.1uF (0402)	1 X 4.7uF (0603) 1 X 1uF (0402)

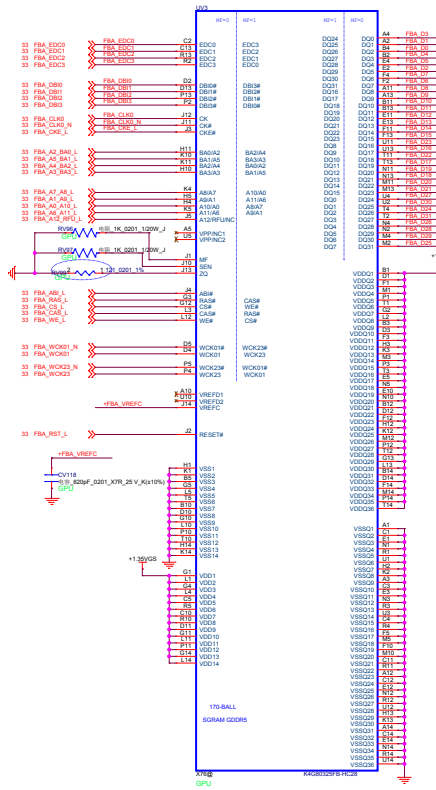
Note:
1. Also see Section 9.2.2.1.10.1



 Huaqin Telecom Technology Co., Ltd.	
Page name: N17S(MEM INTERFACE)	
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Memory - Lower 32 bits



Memory - Upper 32 bits

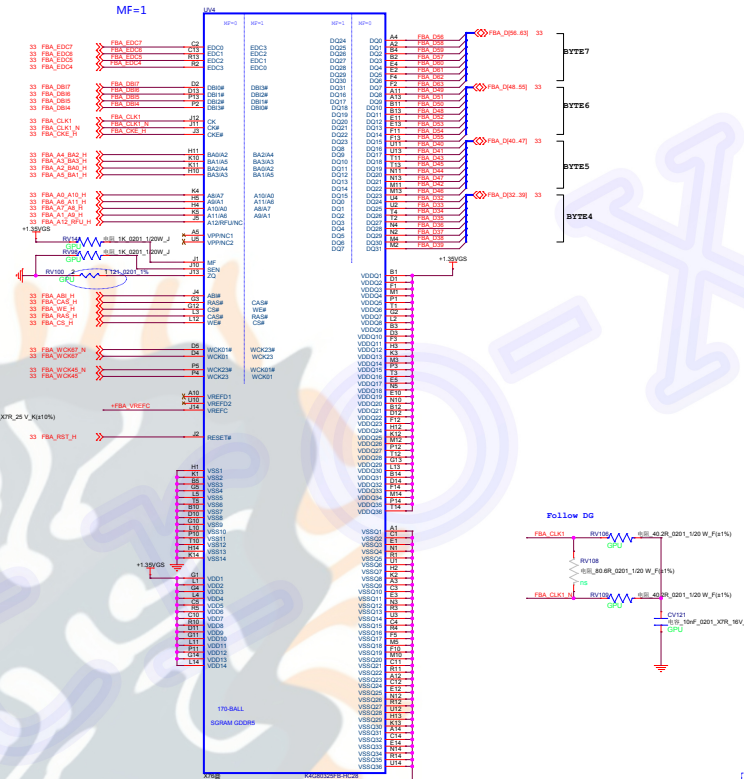
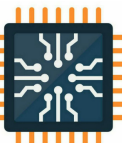
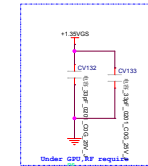
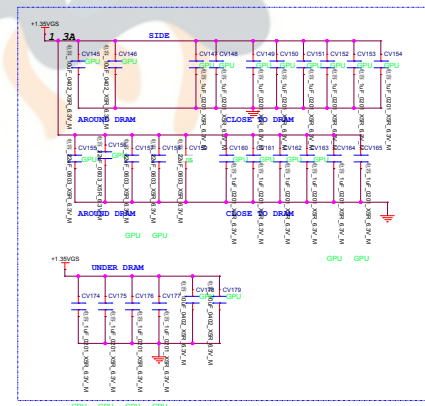
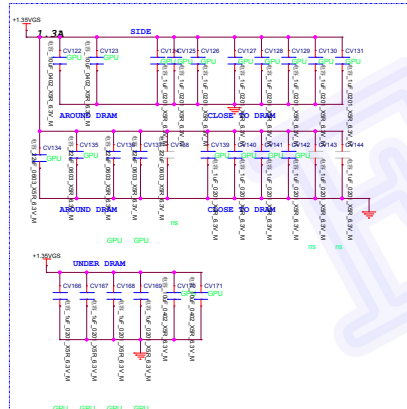
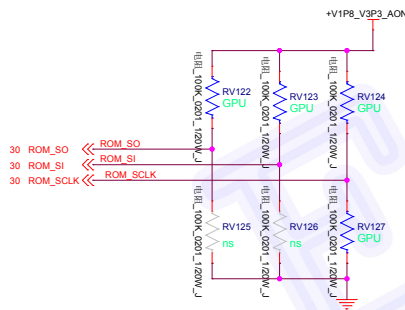
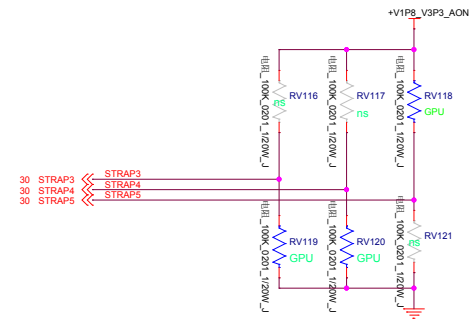
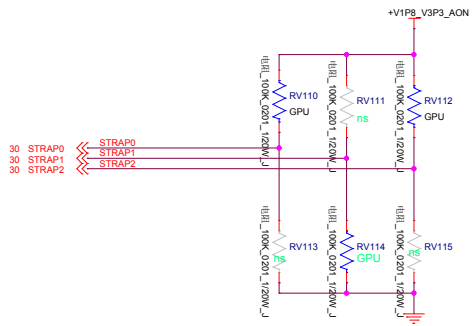


Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (by DRAM Interface Mode)
Combined FBVDD-FBVDDQ Rail			
1.0 uF	X6S [0402]	10	For x32 DRAM: Under the DRAM FBVDD or FBVDDQ ball.
10 uF	X6S [0603]	4	For x16 DRAM in a "shell" PCB configuration: As close to DRAM periphery as possible. Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor.
1.0 uF	X6S [0402]	8 additional	For x32 DRAM: Choose x32 interface to achieve max POR DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDD/Q ball via if possible. See Figure 9.23 for an example.
10 uF	X6S [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X6S [0603]	5	For 4 GHz WCK (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.





For N17

GPU	Vendor	Manufacturer	Strap	Strap2	Strap1	Strap0
N17S-G1	Samsung	K4G80325FB-HC28	0x0	L	L	L
	Micron	MT51J256M32HF-70:A	0x1	L	L	H
	Hynix	H5GC8H24MJR-ROC	0x2	L	H	L
	Micron	MT51J256M32HF-70:B	0x4	H	L	L
N17S_G0/G2	Hynix	H5GC8H24AJR-ROC	0x5	H	L	H
	Micron	MT51J256M32HF-80:B	0x9	L	M	L
	Hynix	H5GC8H24AJR-R2C	0xA	L	M	H

PN	MPN	STRAP	Vendor
HQ11121499000	K4G80325FB-HC28	0x00	Samsung
HQ11121497000	H5GQ8H24MJR-R4C	0x02	Hynix

Physical Strapping pin	Power Rail	RAM_CFG[3]	RAM_CFG[0x02]	RAM_CFG[1]	RAM_CFG[0x00]
STRAP0			L		L
STRAP1			H		L
STRAP2			L		L

SMBUS_ALT_ADDR
0 0x9E (Default)
1 0x9C (Multi-GPU usage)

DEVID_SEL
0 (Default)
1

PCIE_CFG
0 (Default)
1

VGA_DEVICE
0 3D Device (Class Code 302h)
1 VGA Device (Default)

Physical Strapping pin	Power Rail	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SCLK	M				
ROM_SI	H	Disable	Disable	Disable	Disable
ROM_SO	H				

Table 5.3 RAMCFG

Strap Pins <small>see Note</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

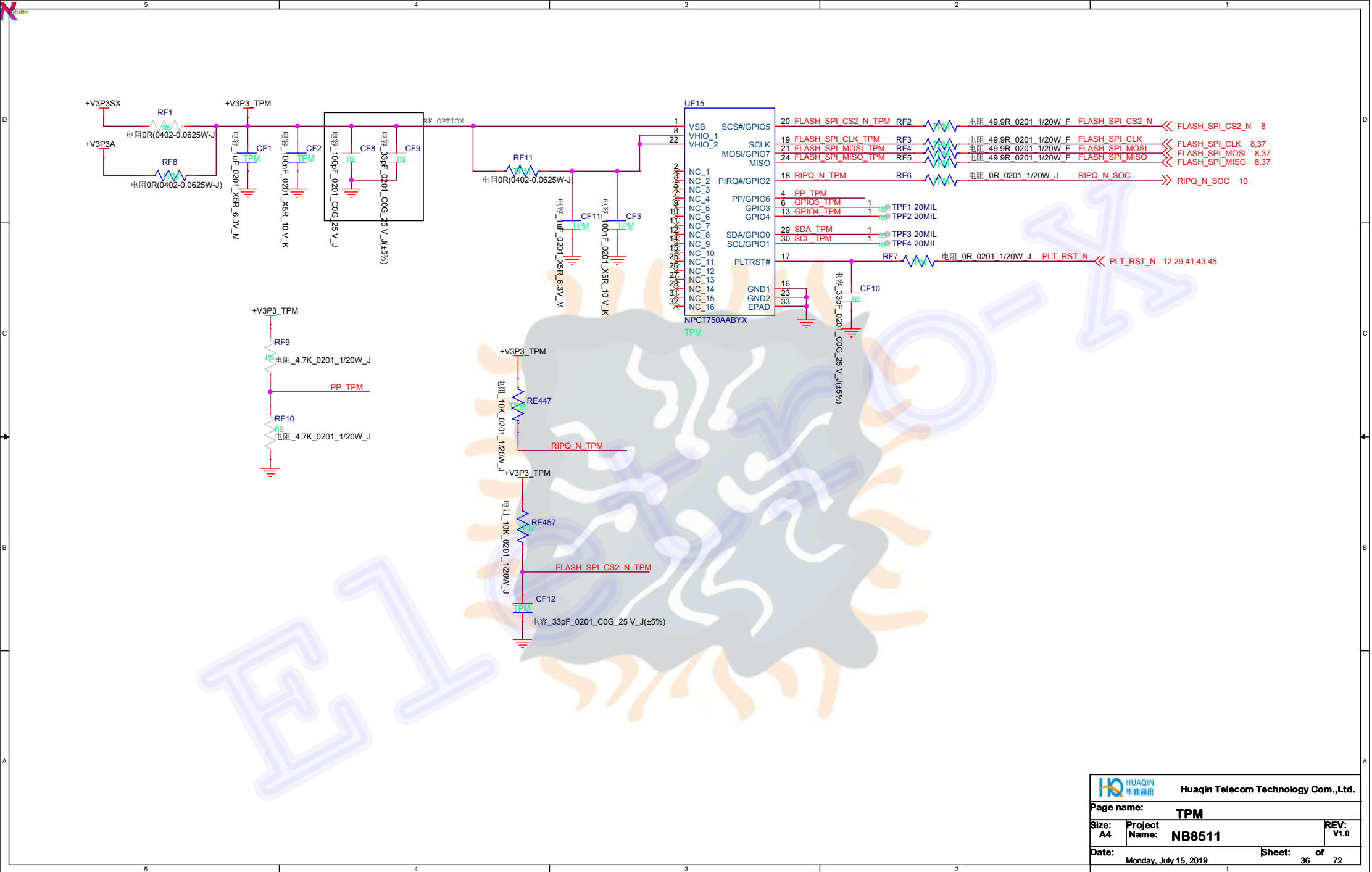
Table 5. N17S-G0/G2 GDDR5 Recommended Memories


Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

Notes:

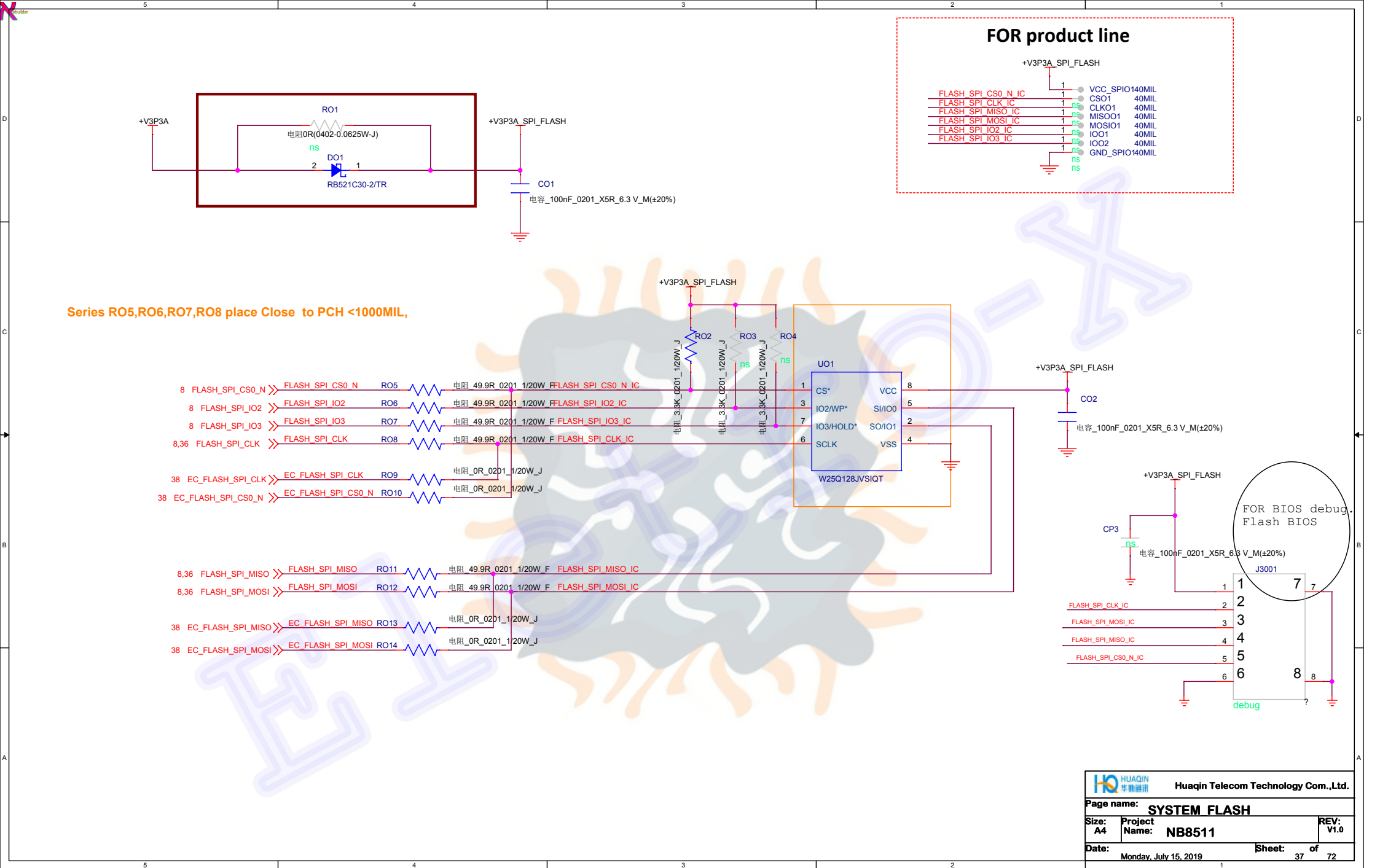
- For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
- N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

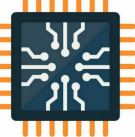
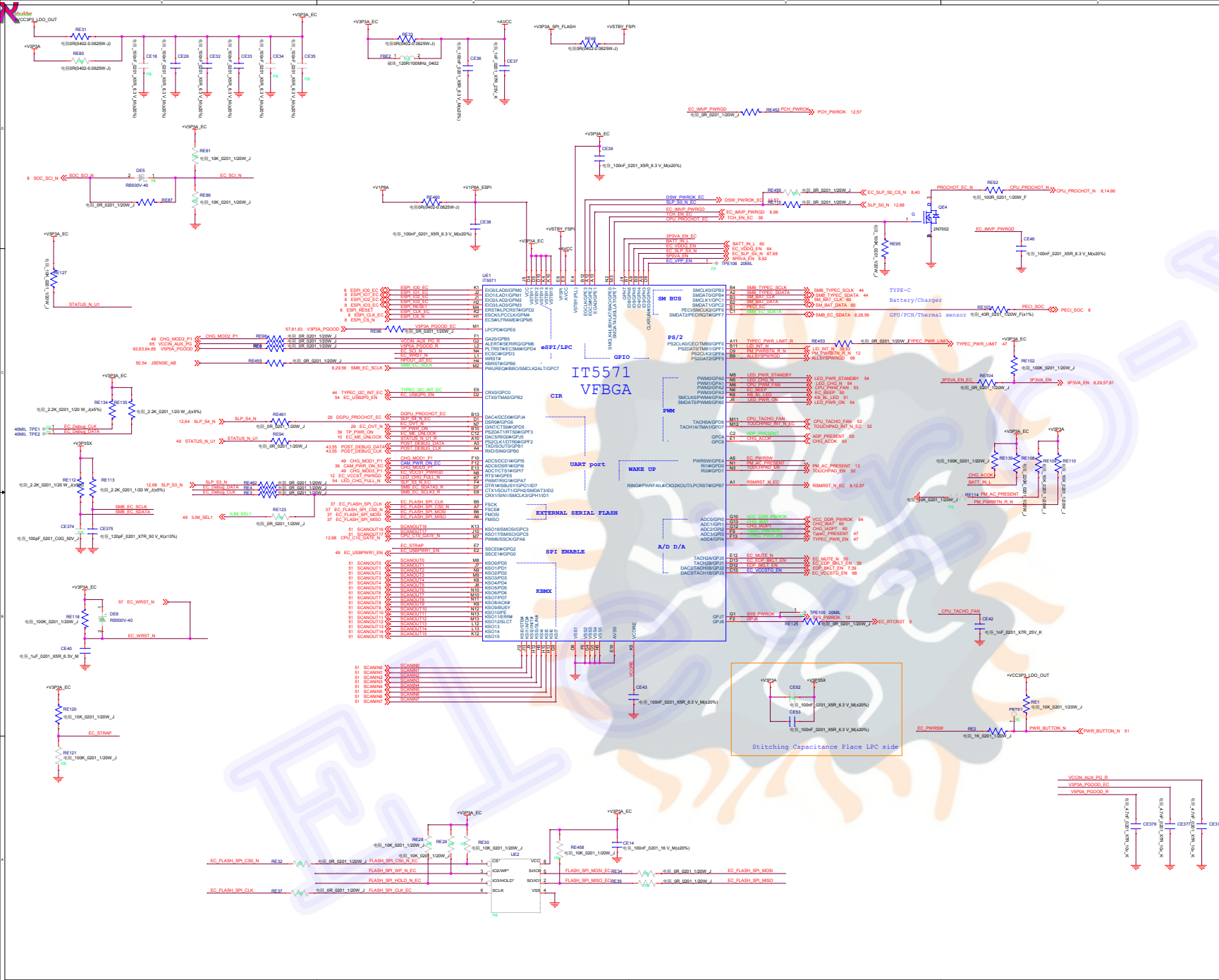




		Huaqin Telecom Technology Com.,Ltd.	
Page name: TPM			
Size: A4	Project Name: NB8511	REV: V1.0	
Date: Monday, July 15, 2019	Sheet: 36	of 72	







[illegible]

电容量: 100nF_0201 X5R 6.3V_M(±20%)

电容量: 2.2uF_0402 X5R_10V_M(±20%)

电容量: 270F_0201_C0G_25V_J

11 USB2_P0_TS_DN

11 USB2_P9_TS_DP

USB2_P9_TS_DP

EXC14CE9000

电阻_OR_0201 1/20W_J

USB2_P9_TS_DP_R

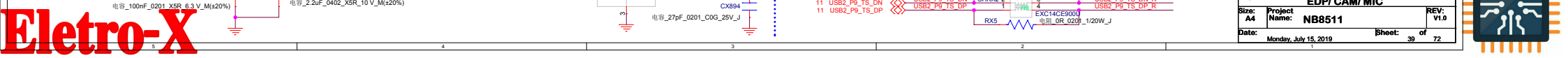
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Project Name: NB8511

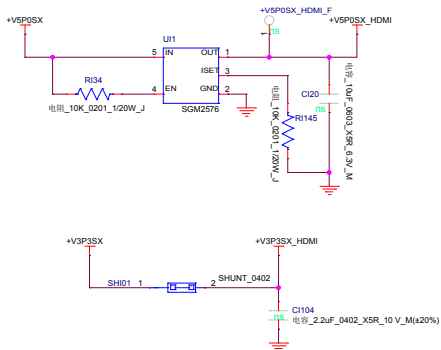
Date: Monday, July 15, 2019

REV: V1.0

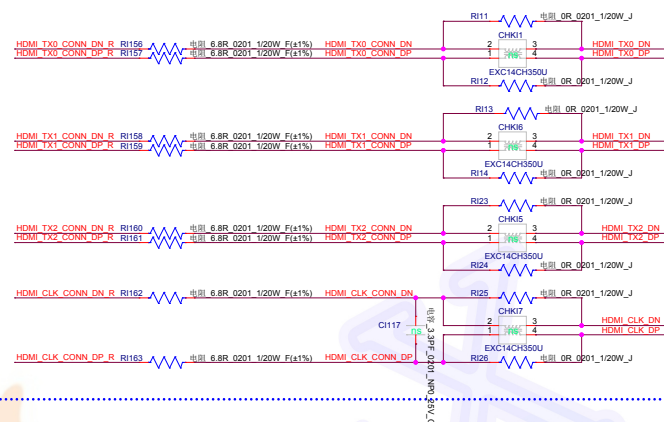
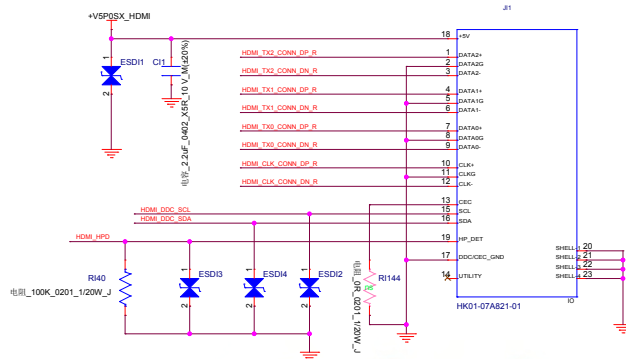
Sheet: 39 of 72



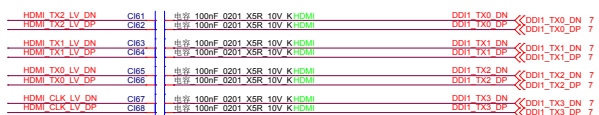
Power 1



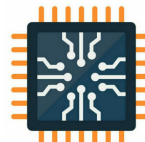
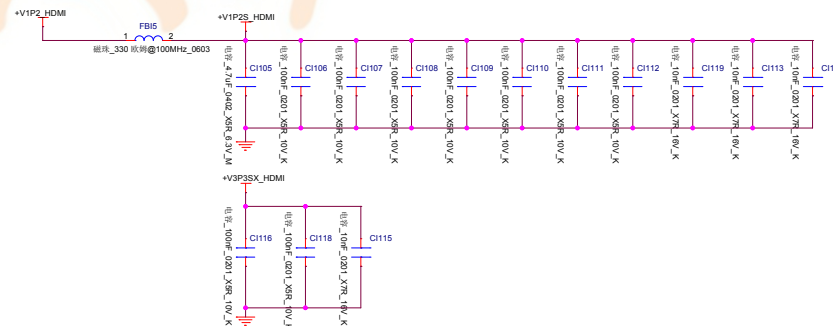
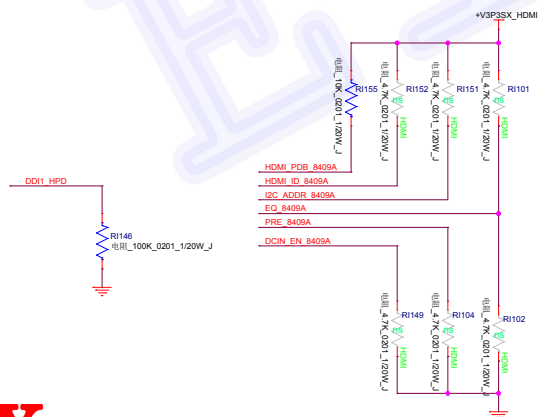
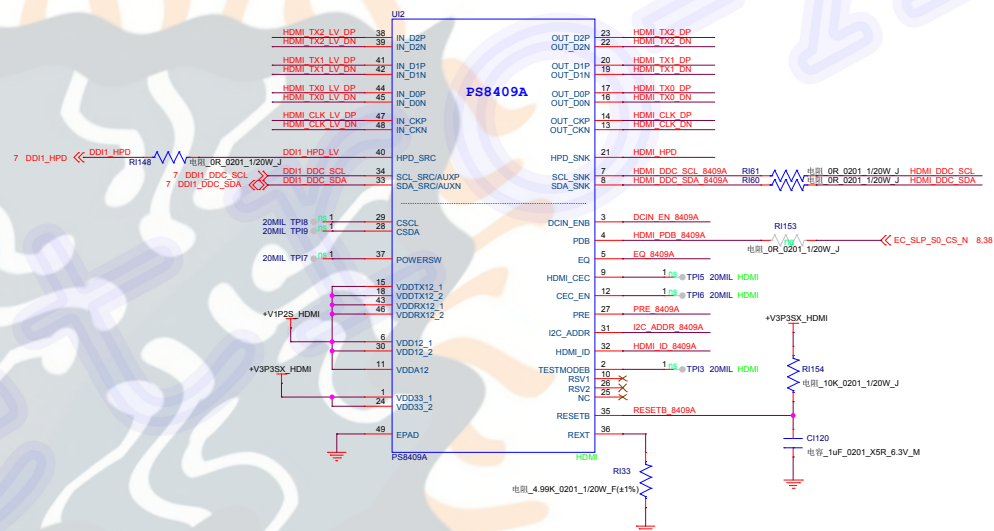
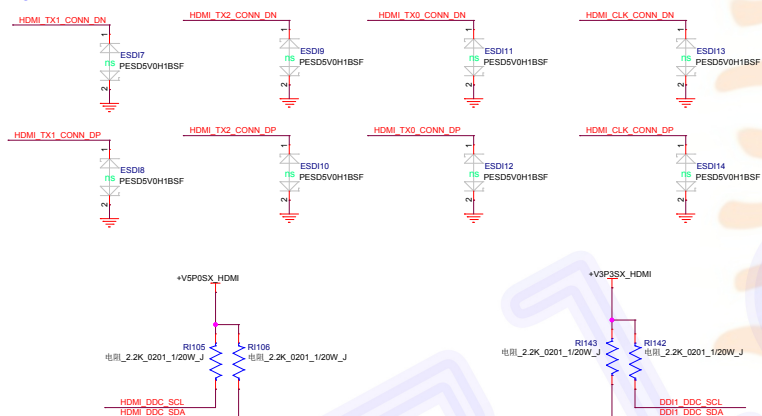
HDMI CONN



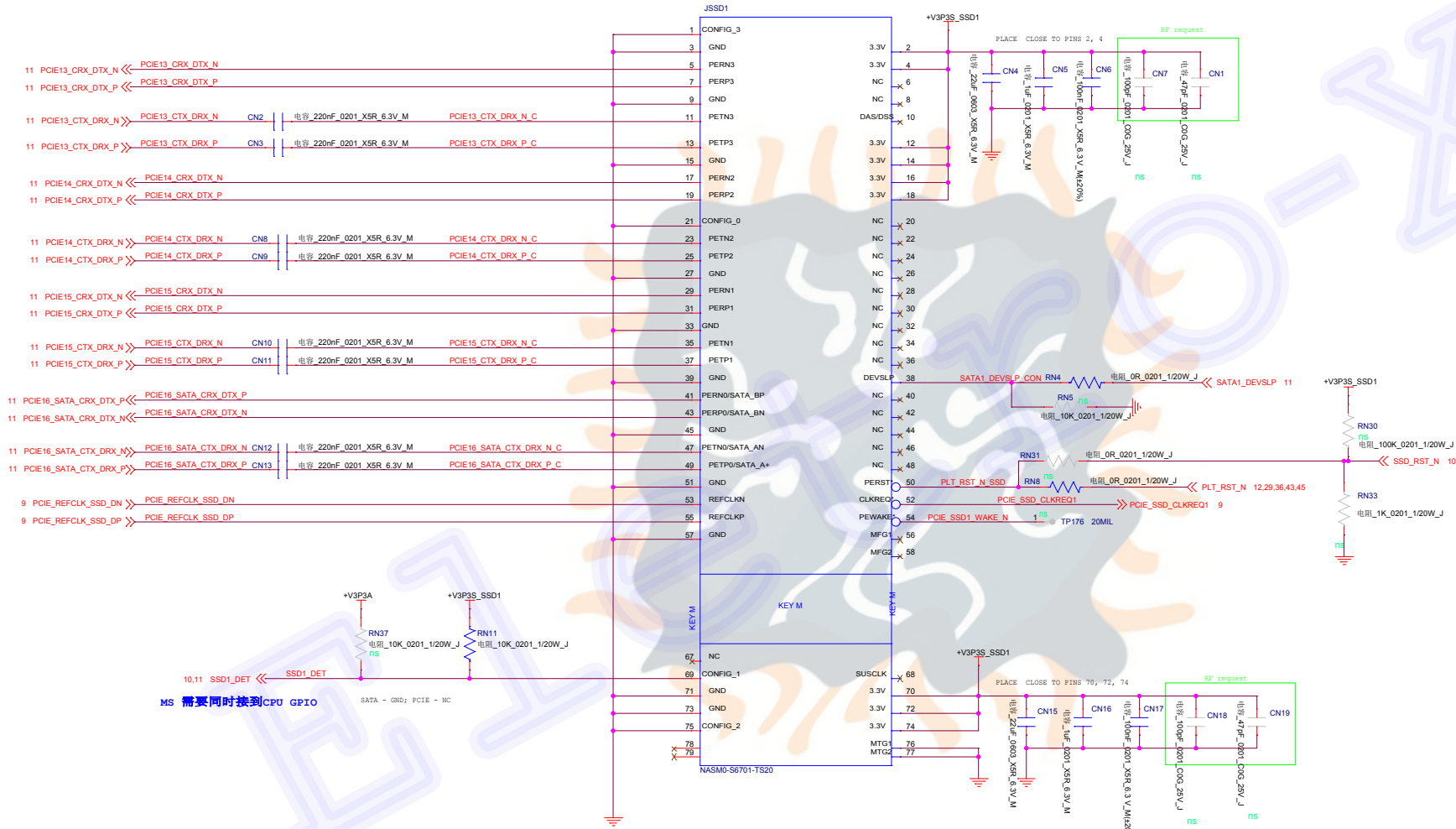
Signal



ESD



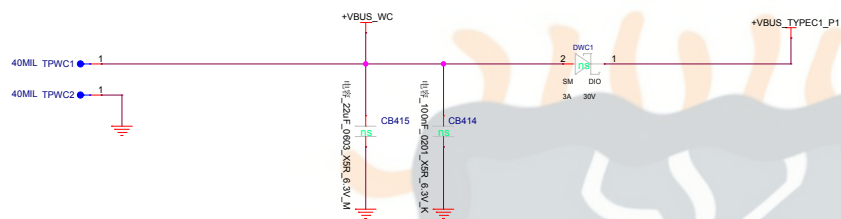
SSD

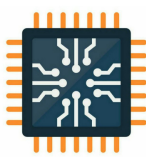


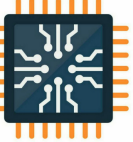
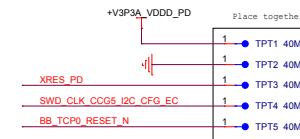
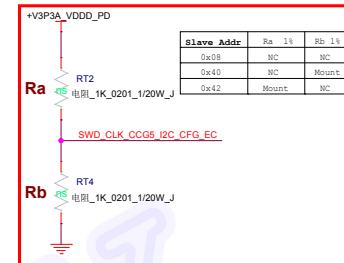
MS 需要同时接到CPU GPIO

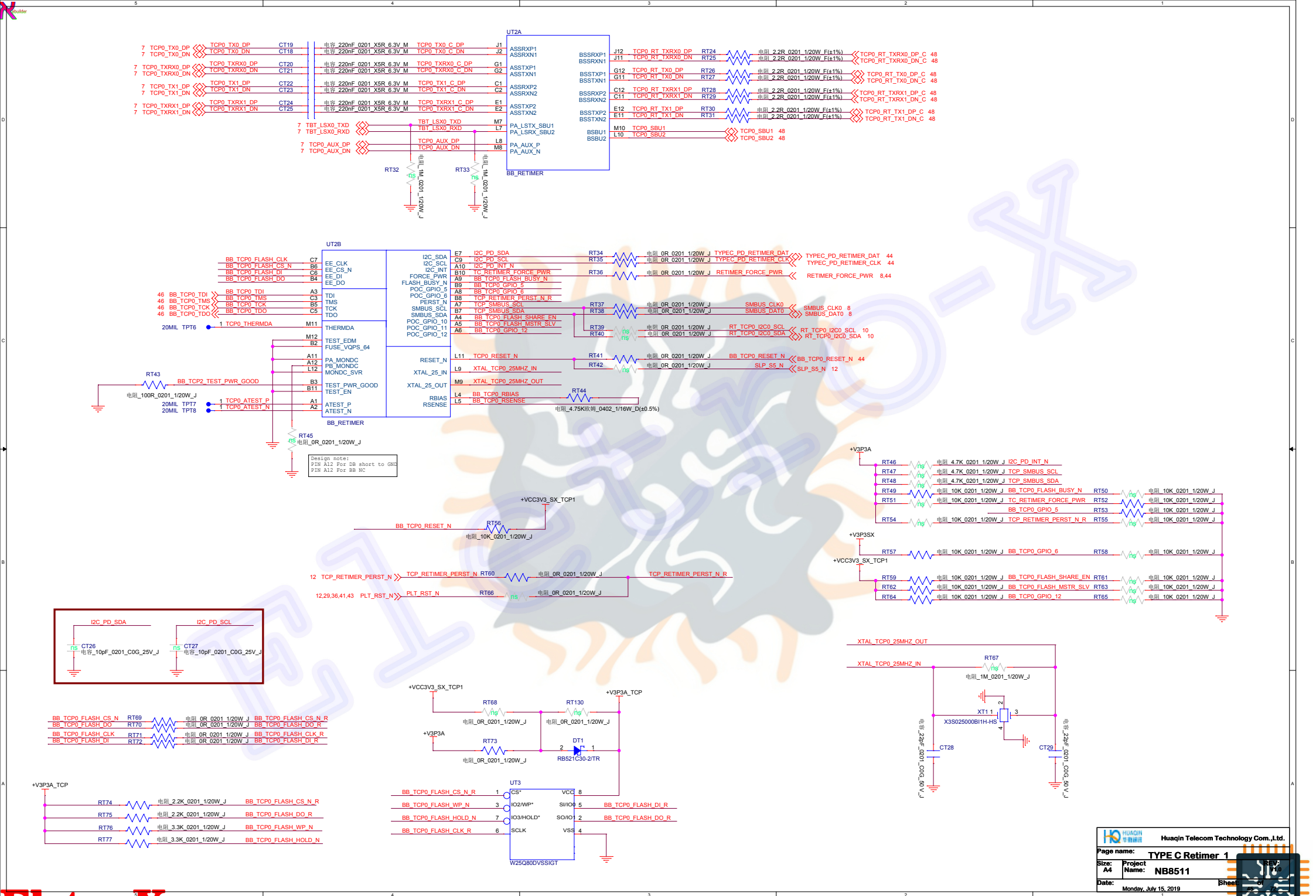
SATA - GND; PCIE - NC





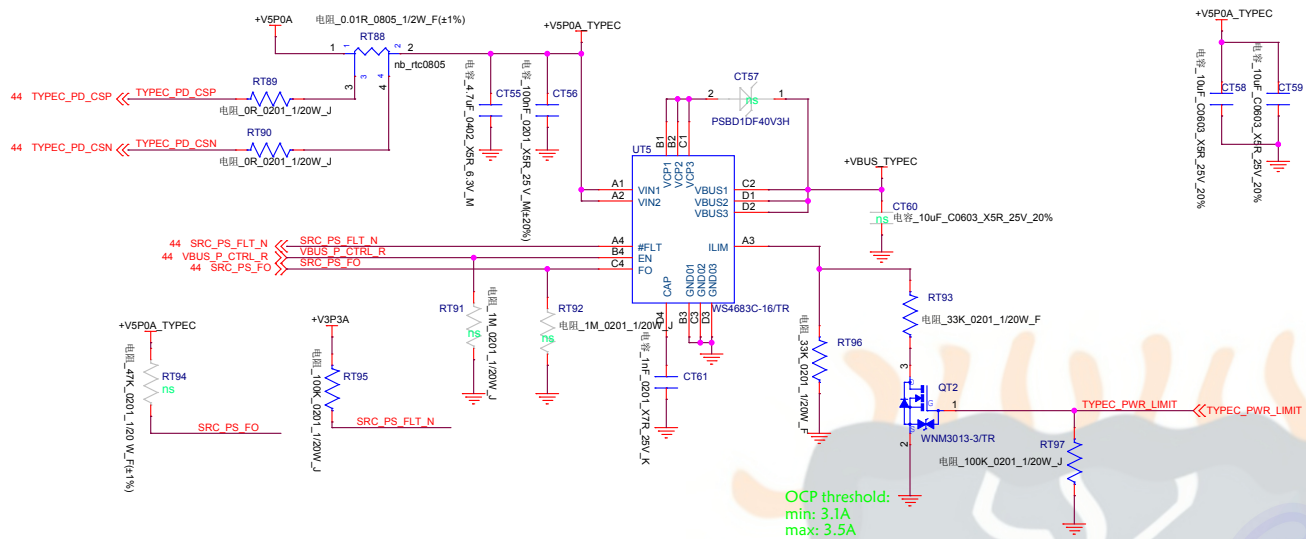




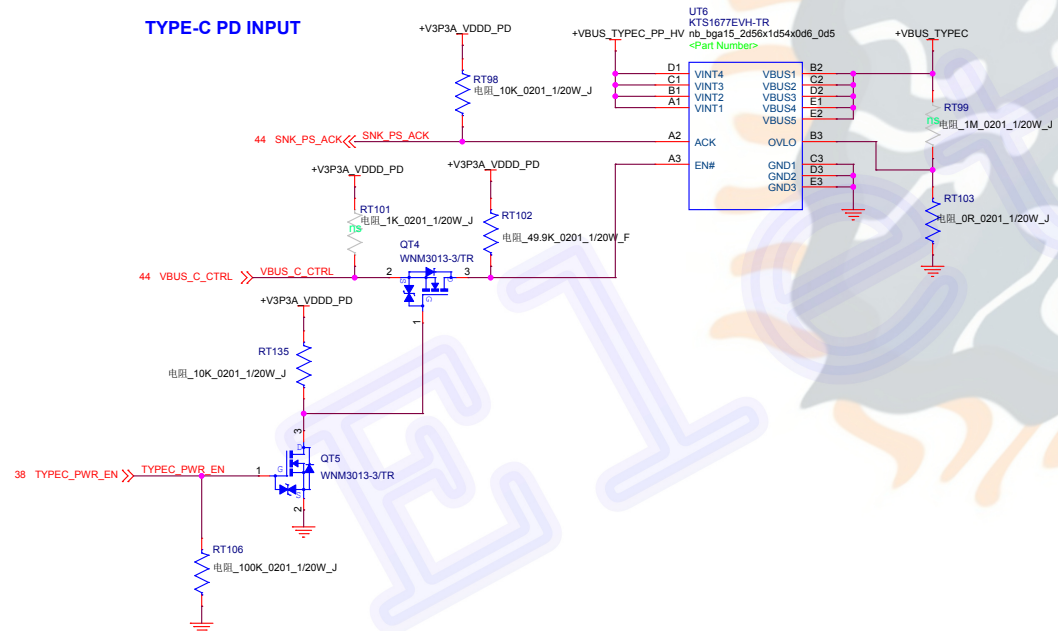




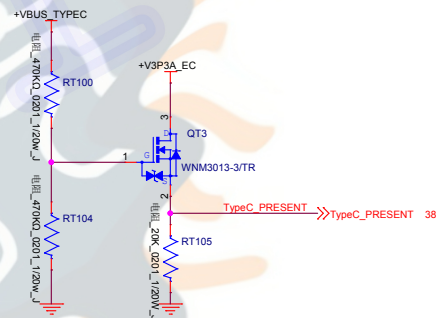
TYPE-C PD OUTPUT



TYPE-C PD INPUT

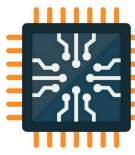


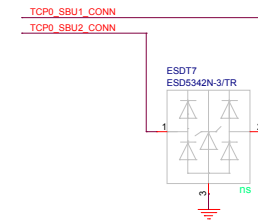
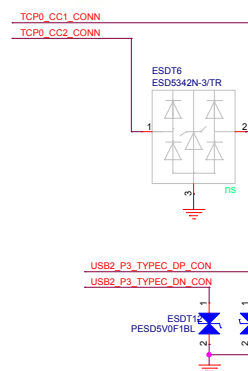
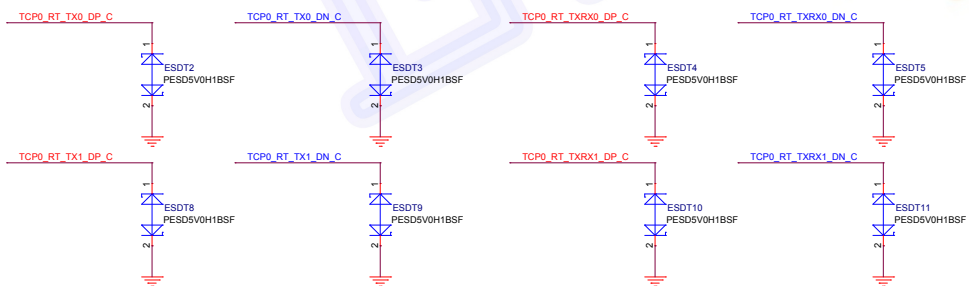
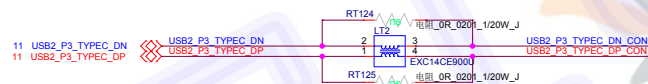
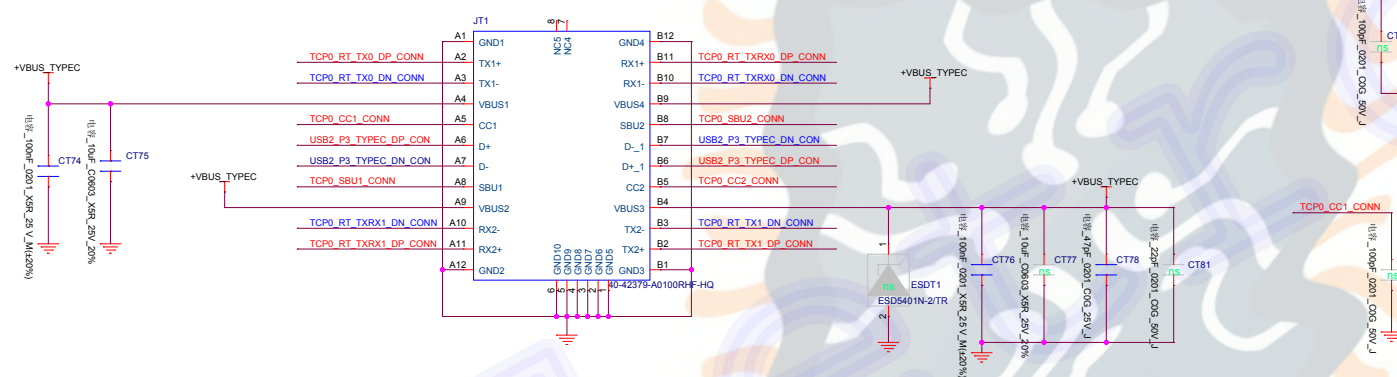
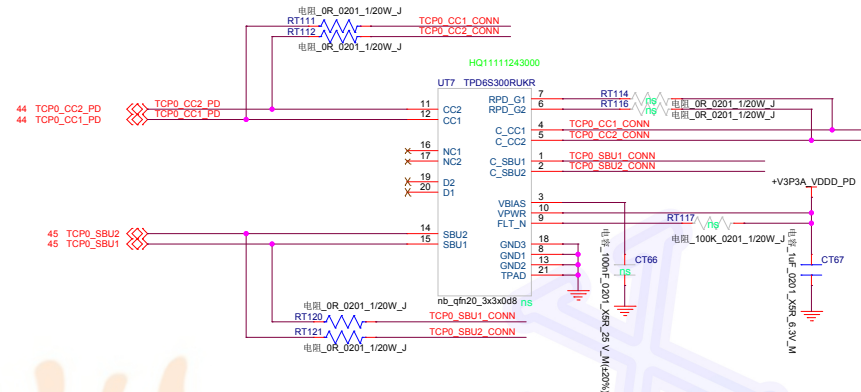
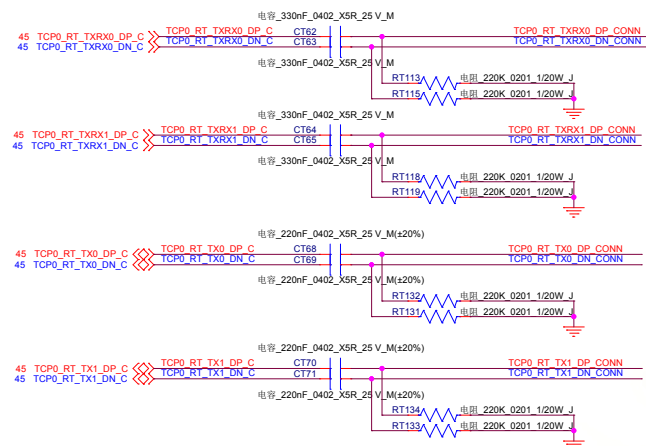
TYPEC-IN detect



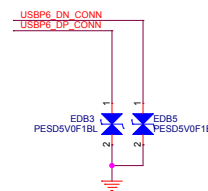
dead battery power on logic

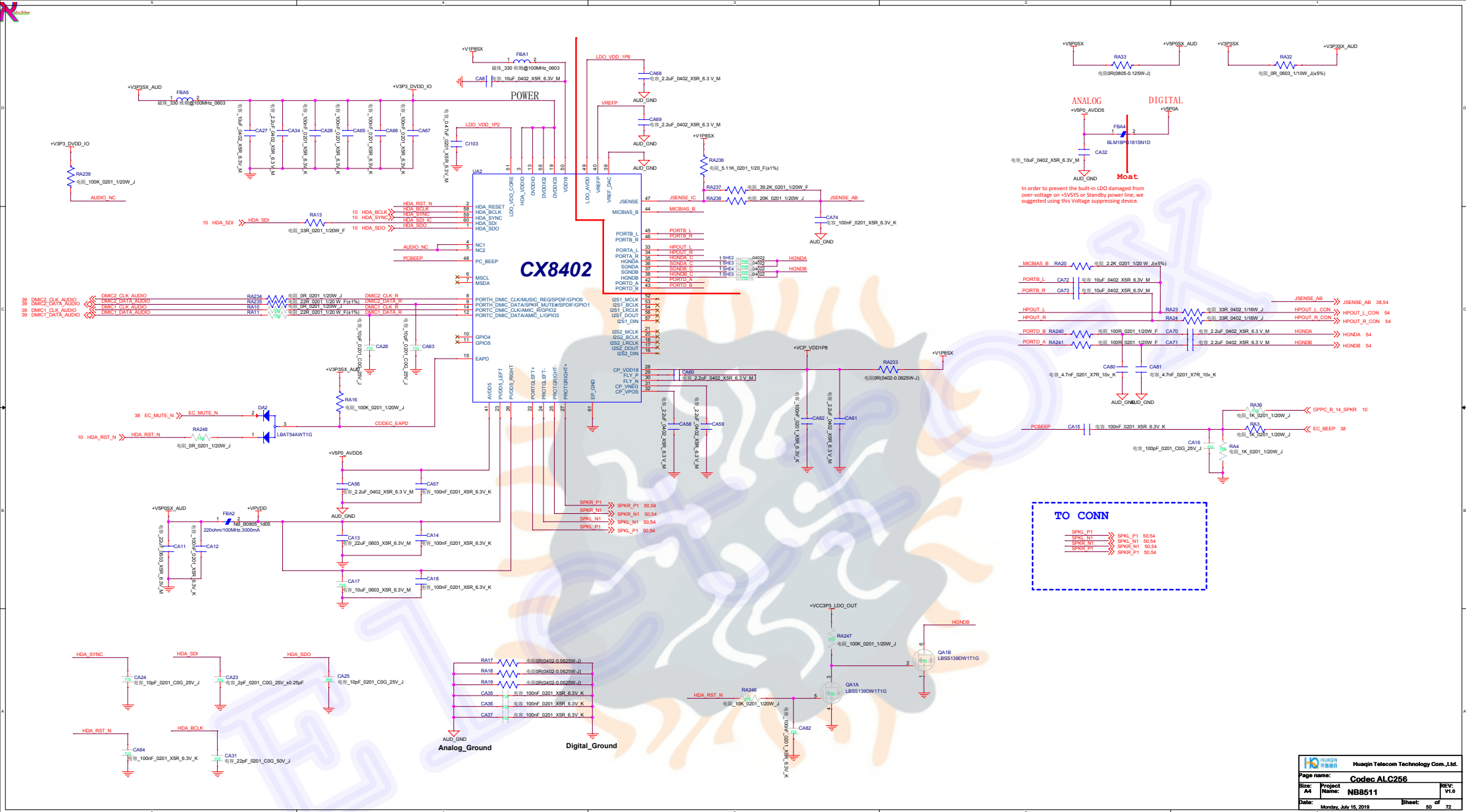
Discharge



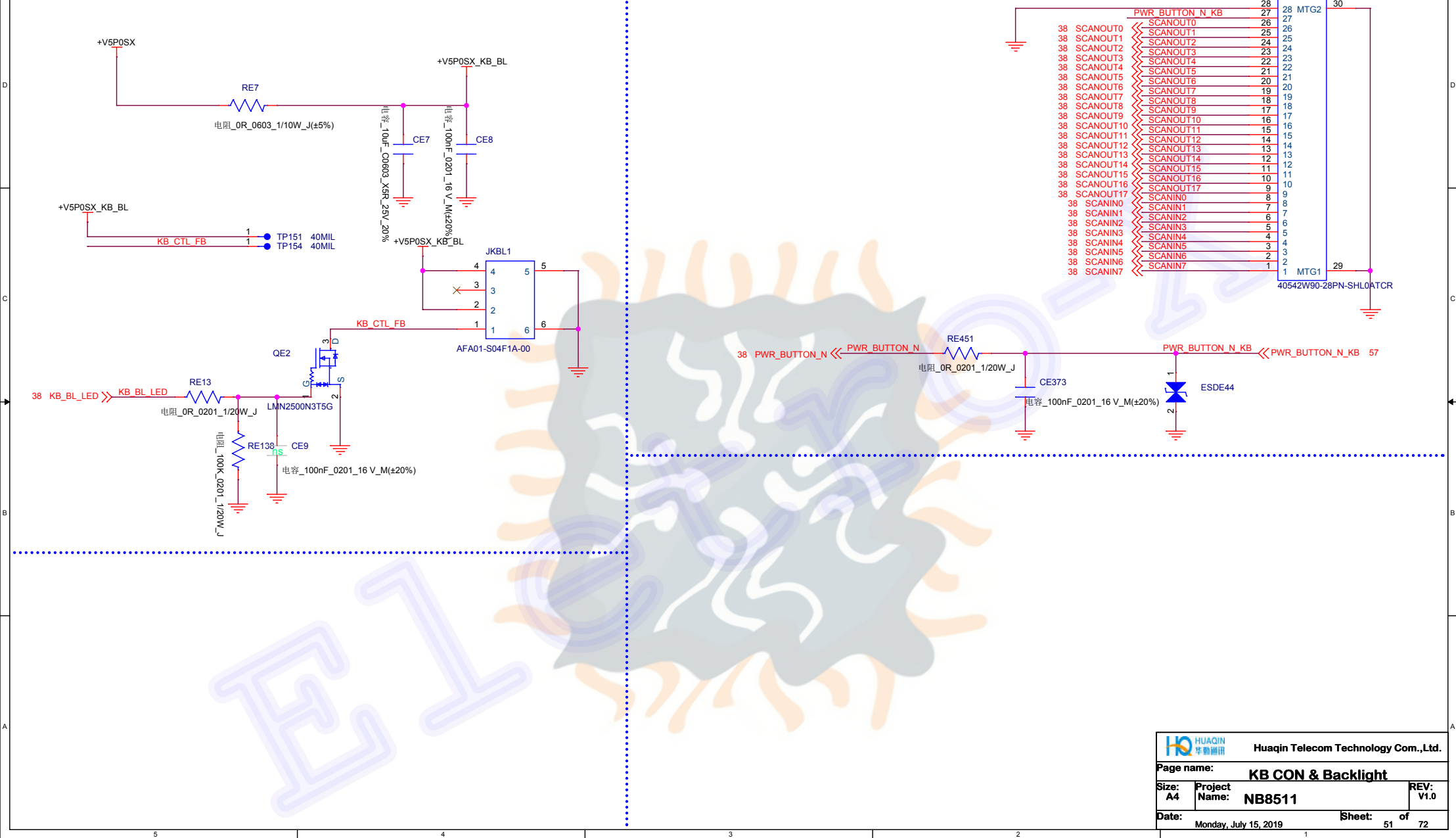


USB3.1 ESD





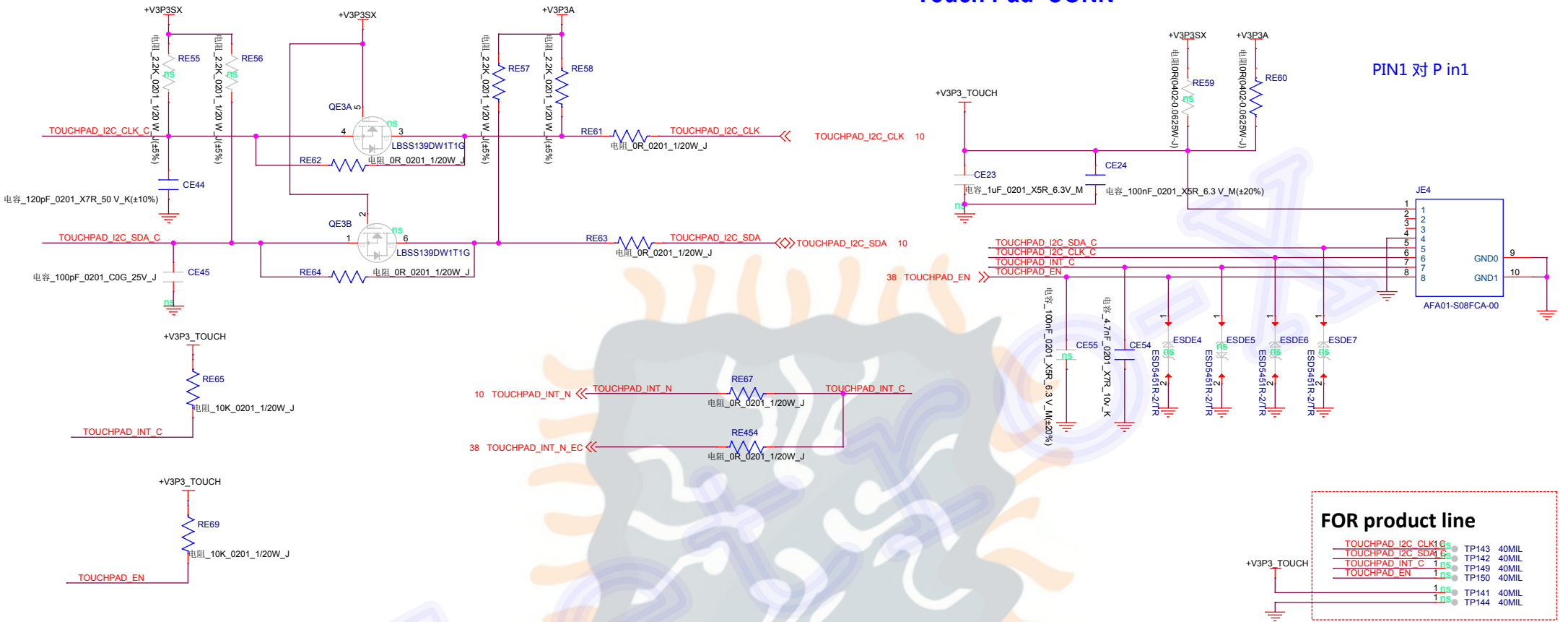
KB CONN



Touch Pad

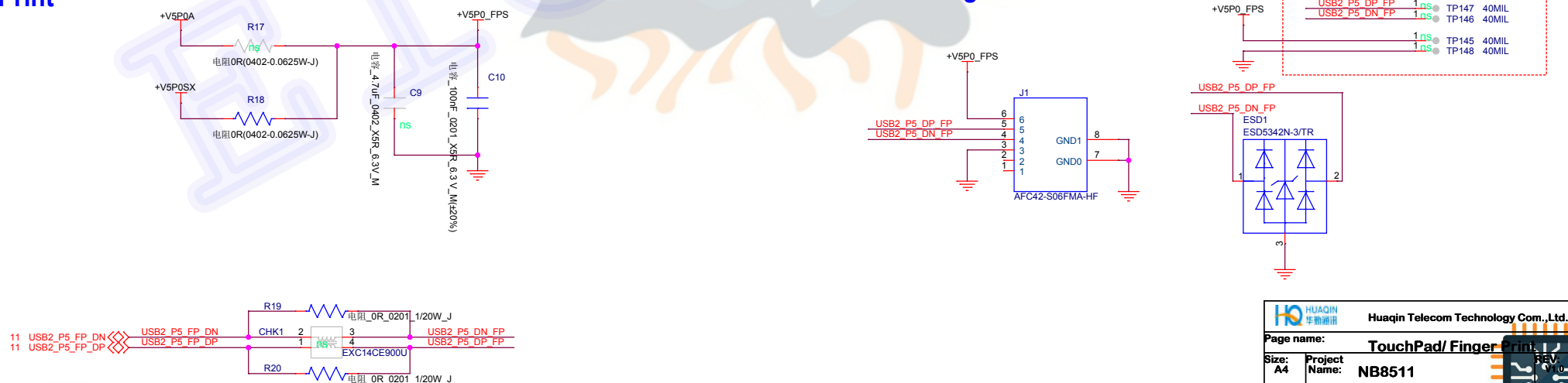
Touch Pad CONN

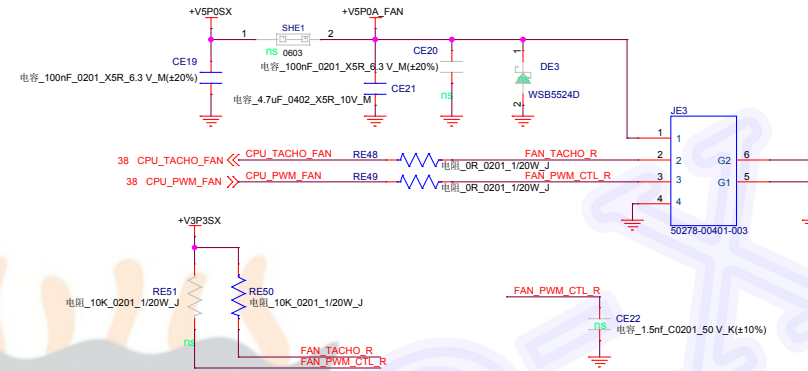
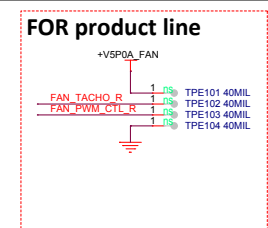
PIN1 对 P in1



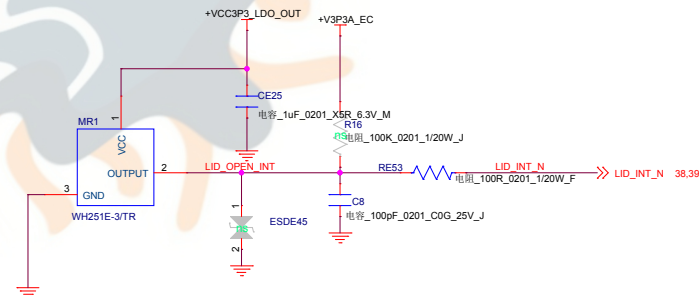
Finger Print

Finger Print CONN

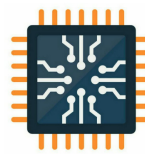


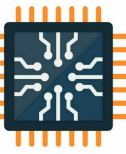
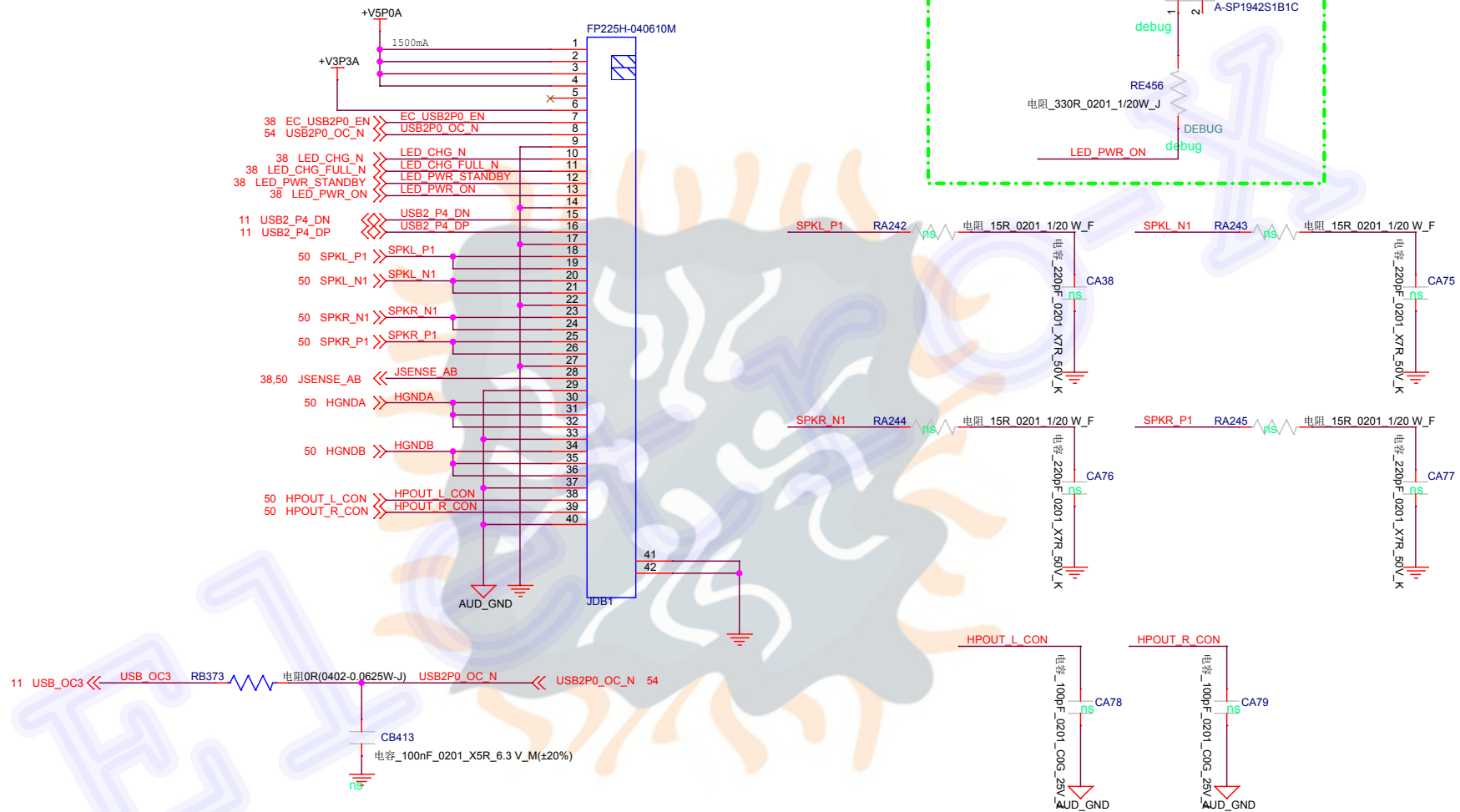


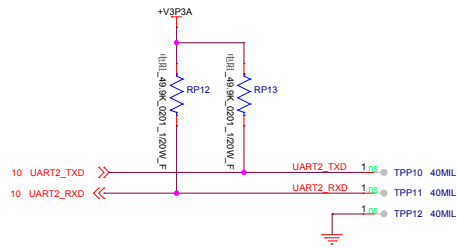
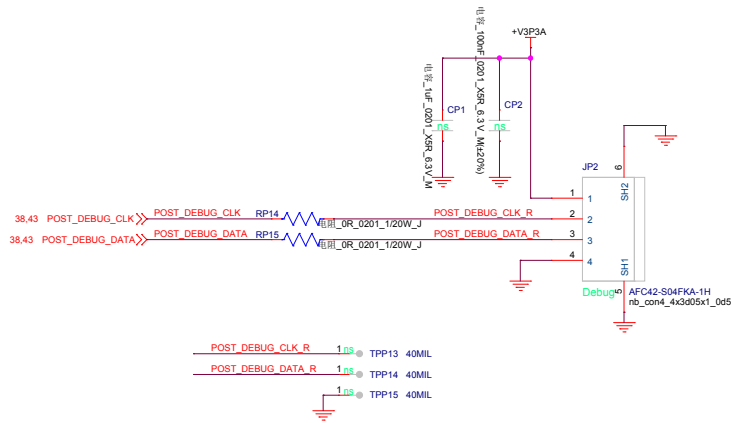
HALL



Huaqin Telecom Technology Com.,Ltd.			
Page name:	G-SENSOR/FAN/LED/Hall		
Size: A4	Project Name:	NB8511	REV: V1.0
Date:	Monday, July 15, 2019	Sheet:	53 of 72

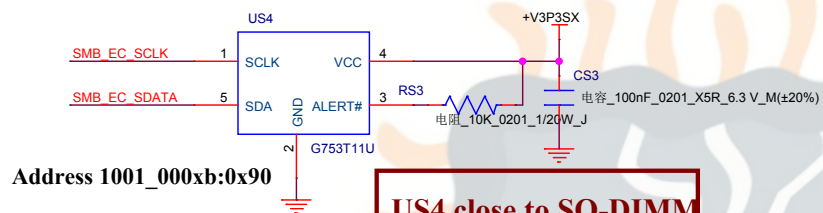
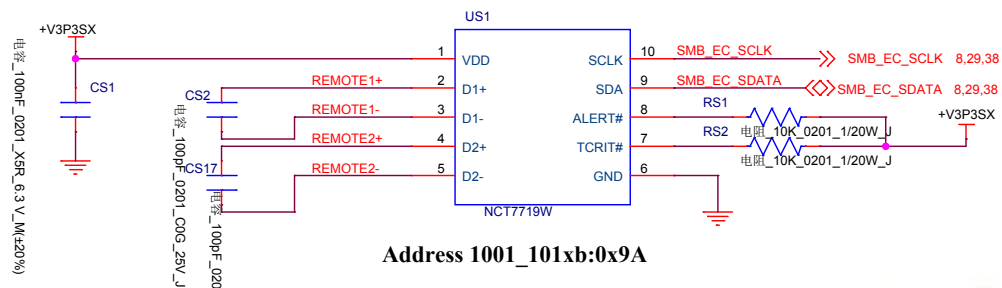




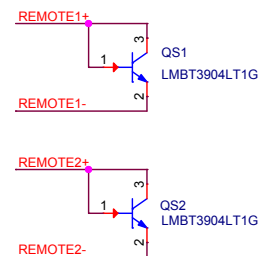


REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"
Connect guard traces to GND on either side of the
DXP-DXN traces


Close to charger

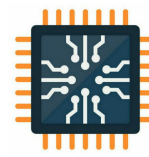


US4 close to SO-DIMM

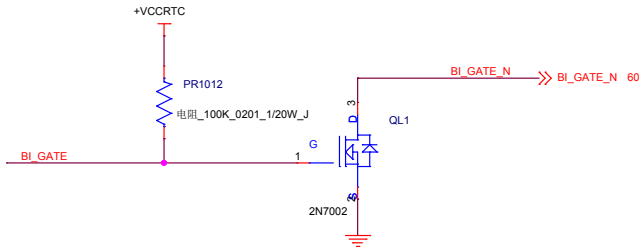
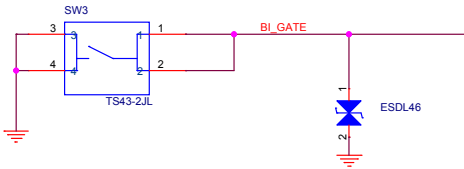


Between CPU and GPU

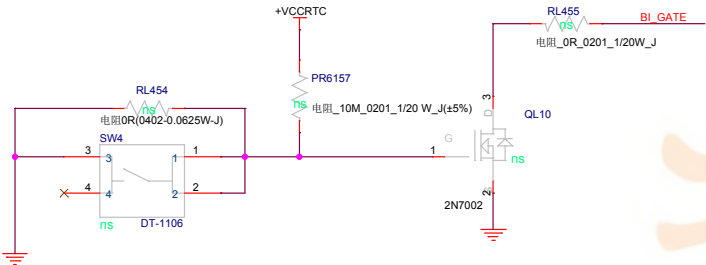
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Page name: Thermal sensor			
Size: A4	Project Name: NB8511		REV: V1.0
Date: Monday, July 15, 2019	Sheet: 56		of 72



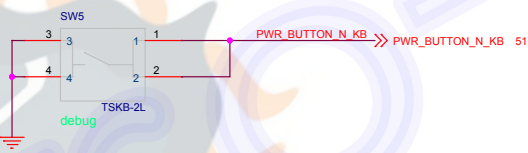
Reset BUTTON



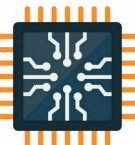
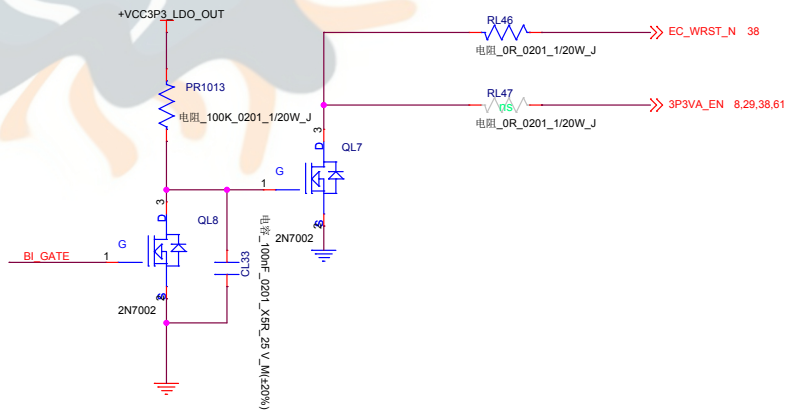
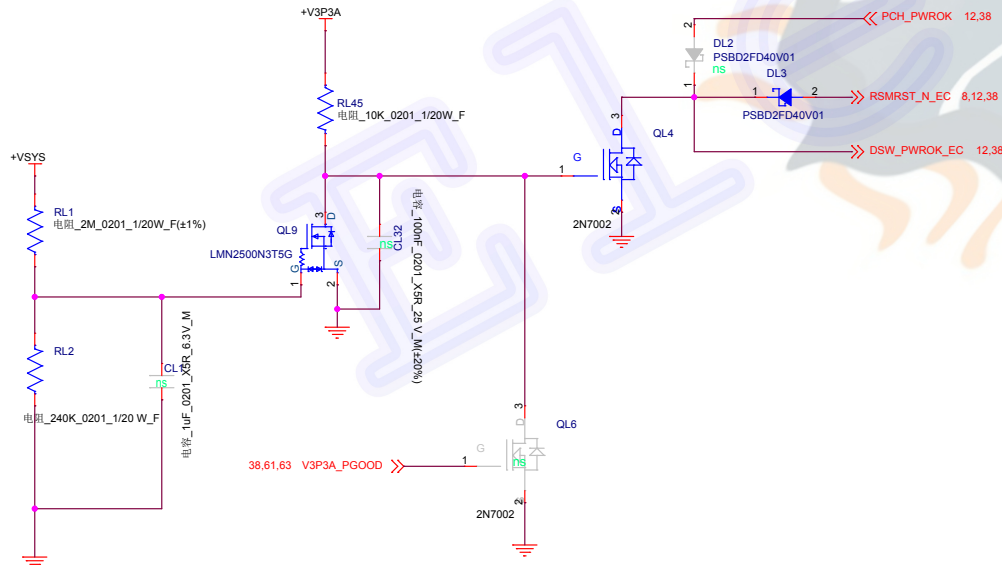
Open door BUTTON

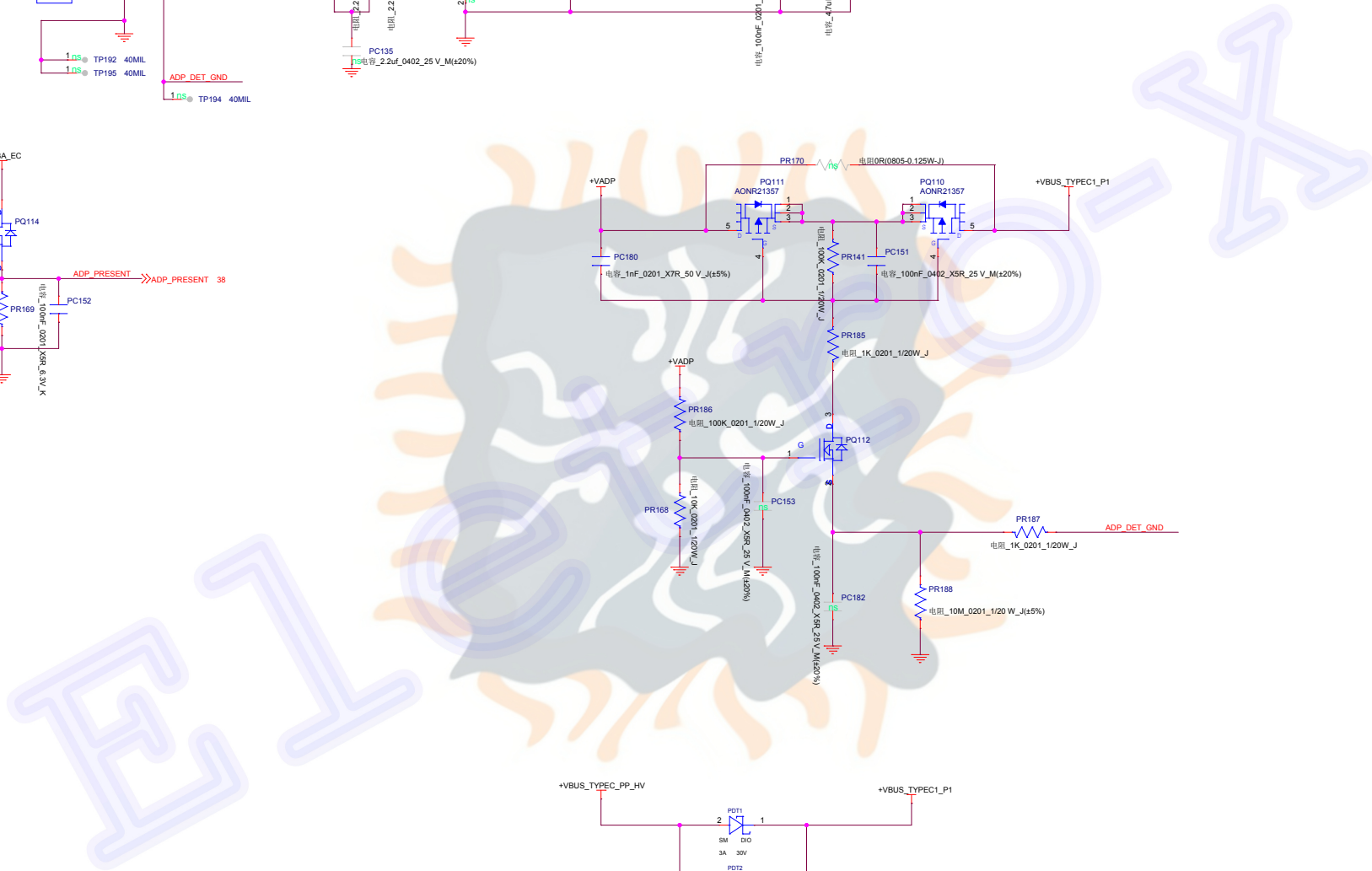


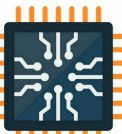
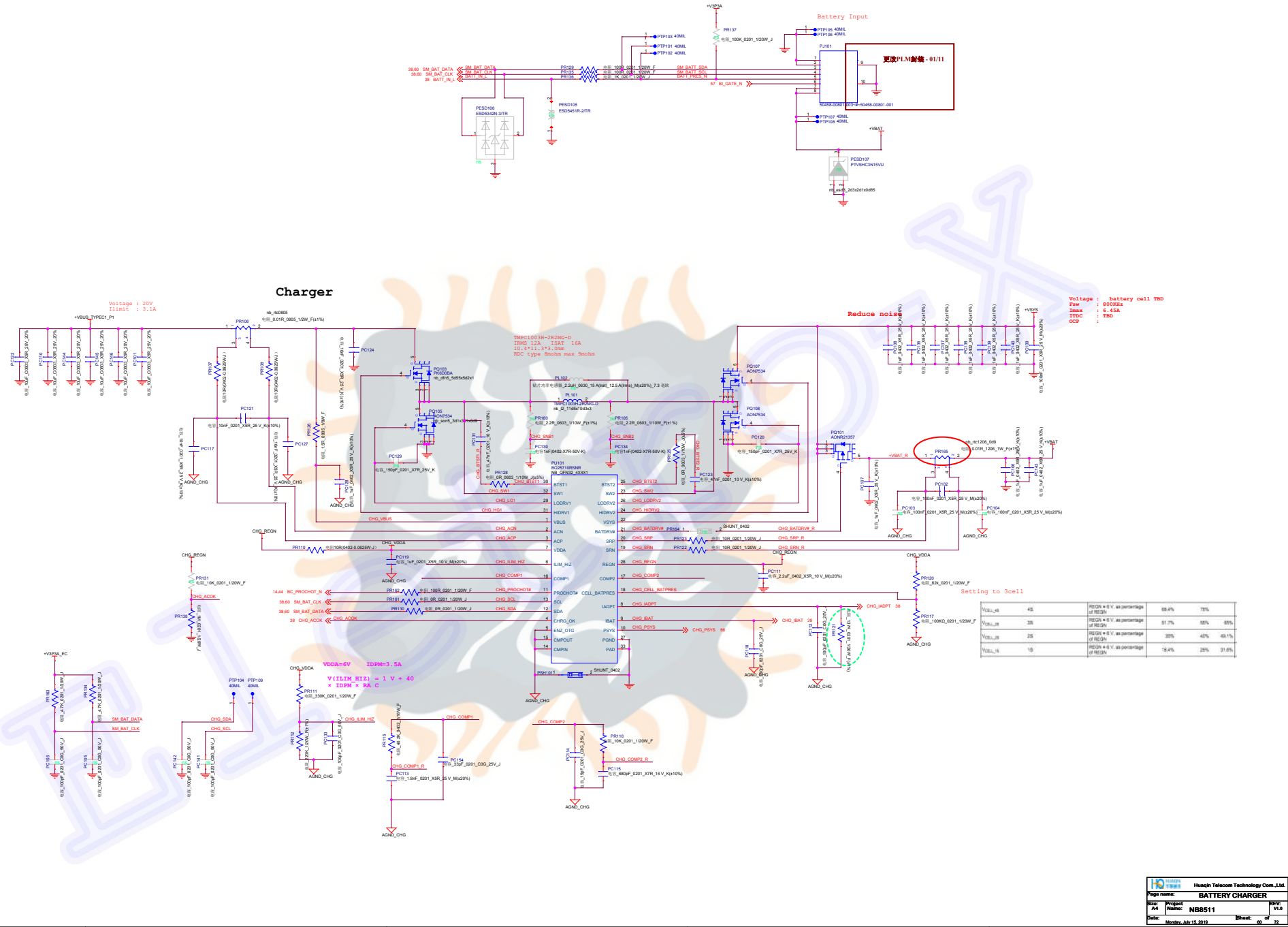
Debug BUTTON

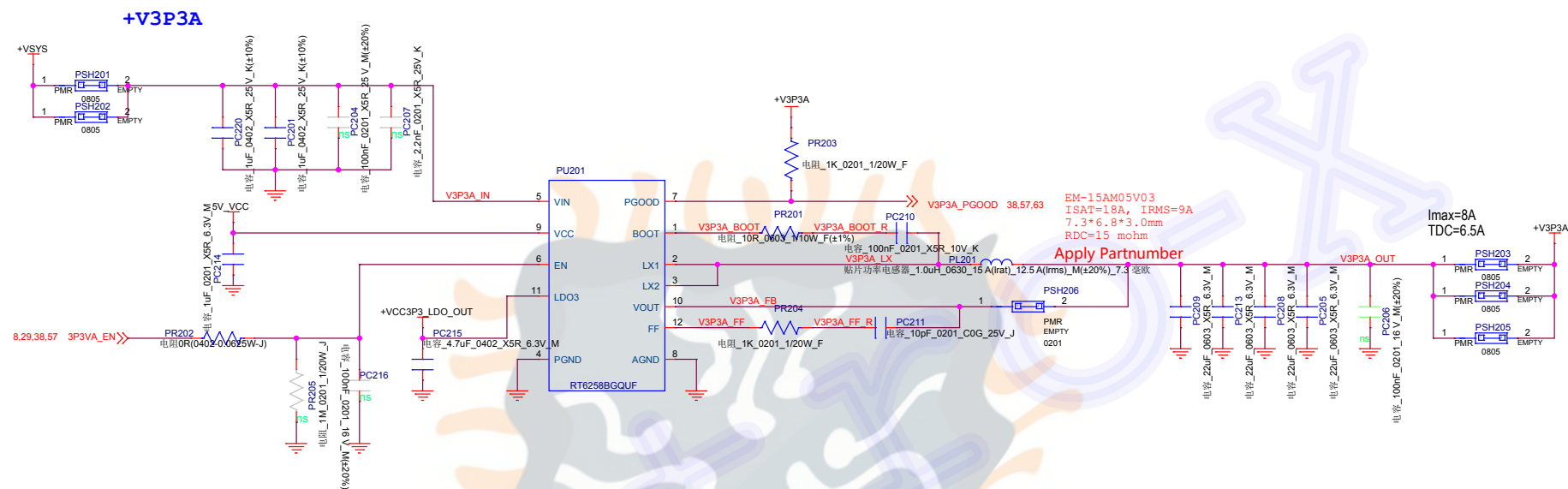


Abnormal PD logic

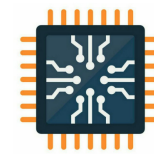


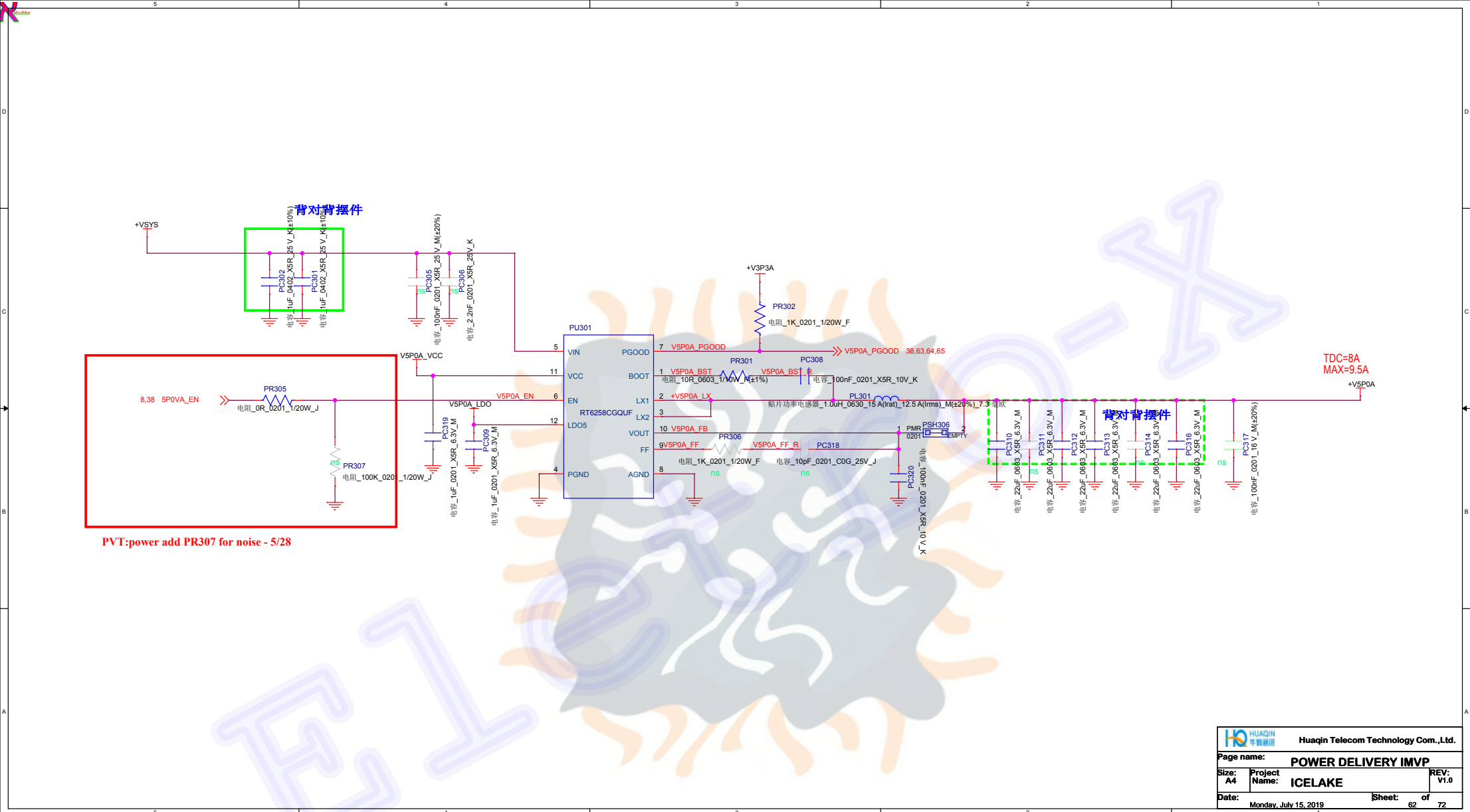







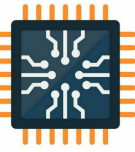
HUAQIN 华勤通信		Huaqin Telecom Technology Com.,Ltd.	
Page name:		POWER DELIVERY 5V 3.3V	
Size: A4	Project Name: ICELAKE	REV: V1.0	
Date: Monday, July 15, 2019	Sheet: 61	of 72	

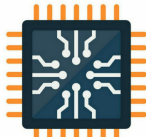
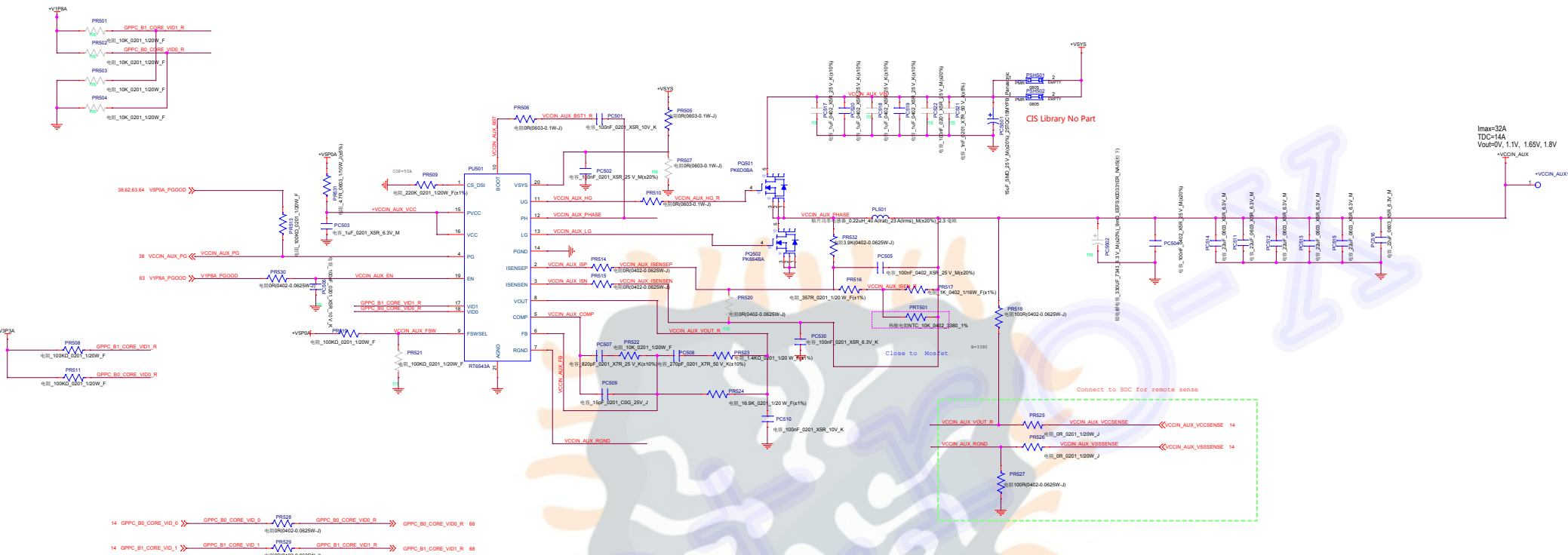


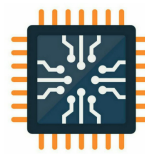
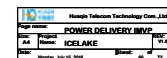


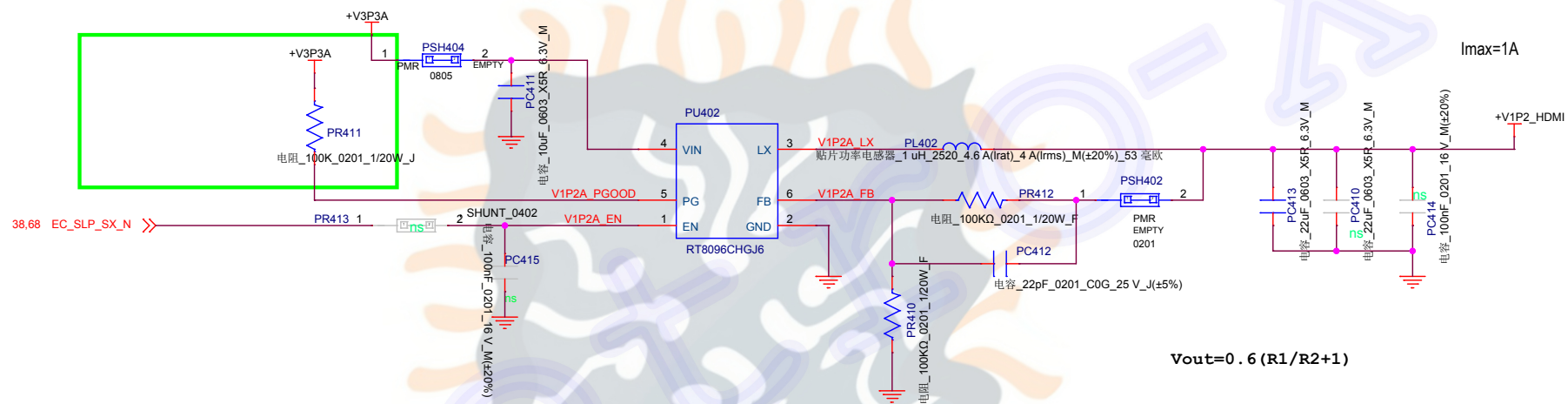
PVT:power add PR307 for noise - 5/28


		Huaqin Telecom Technology Com.,Ltd.	
Page name: POWER DELIVERY IMVP			
Size: A4	Project Name: ICELAKE	REV: V1.0	
Date: Monday, July 15, 2019	Sheet: 62	of 72	

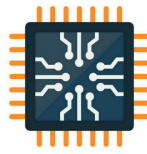


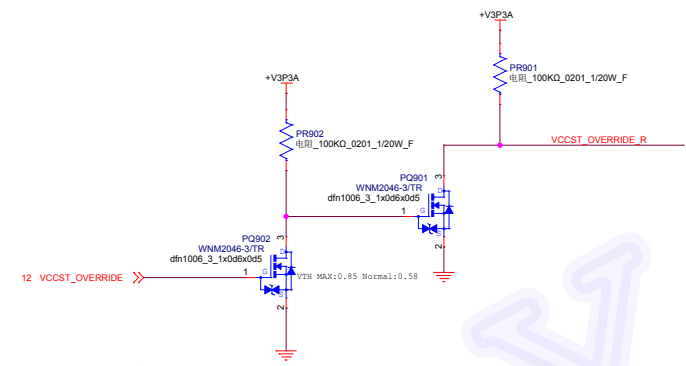
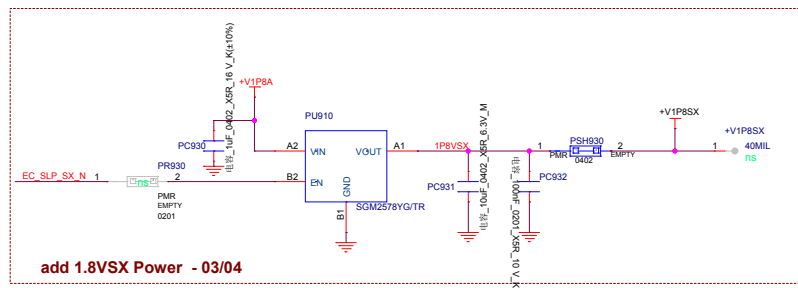




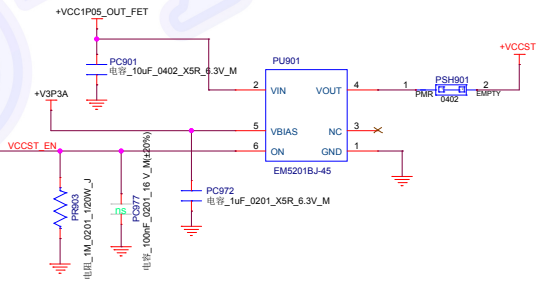
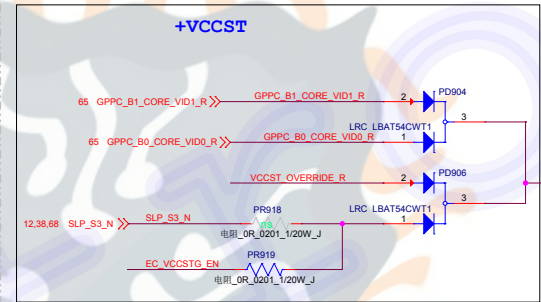
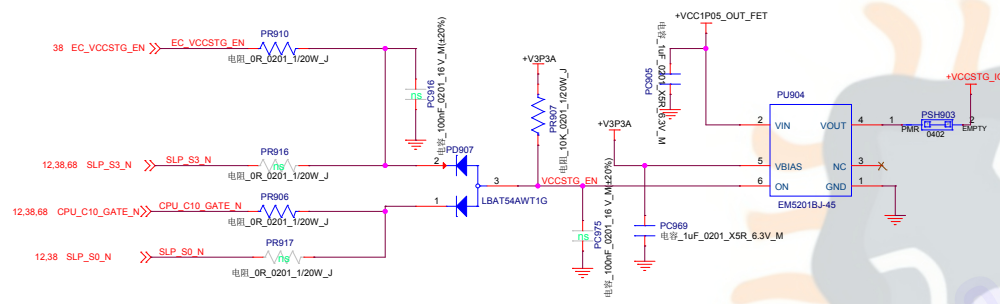


		Huaqin Telecom Technology Com.,Ltd.	
Page name: Hole & Mark			
Size: A4	Project Name: ICL-U42	REV: V1.0	
Date: Monday, July 15, 2019	Sheet: 67	of 72	

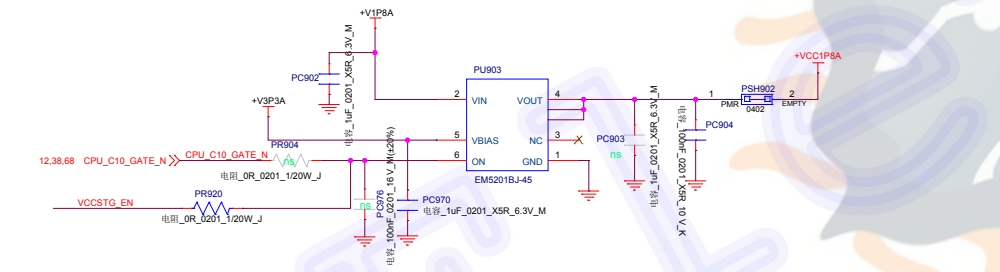




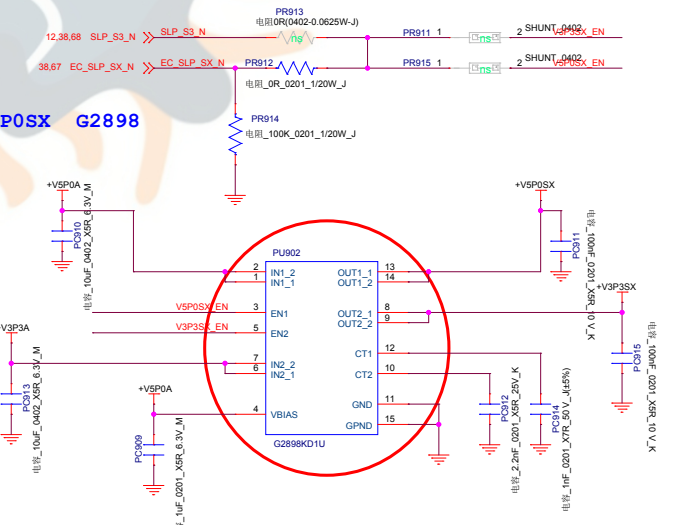
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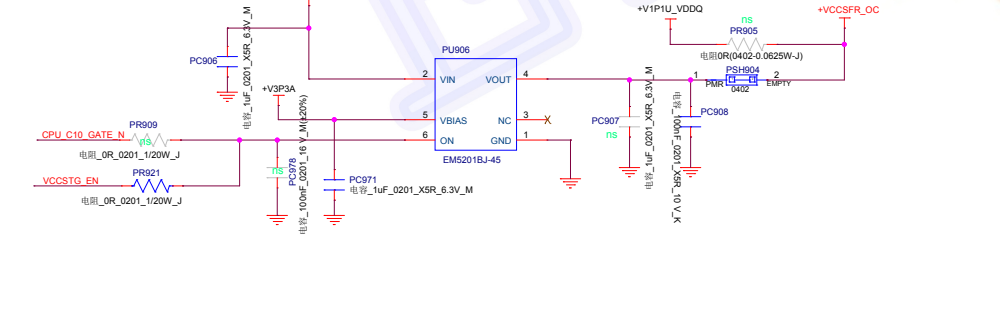
+VCC1P8A



+V3P3SX, +V5P0SX G2898



+VCCSFR_OC



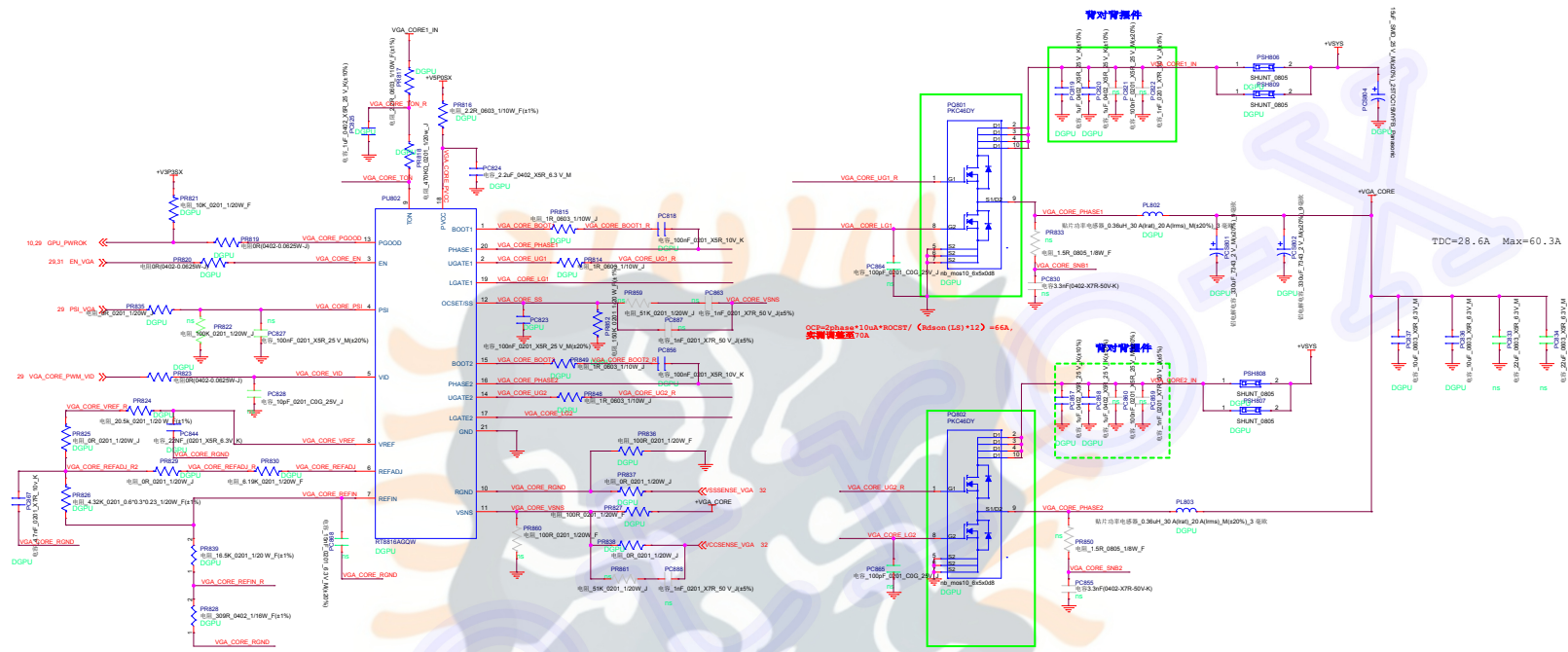


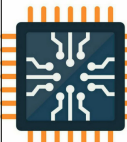
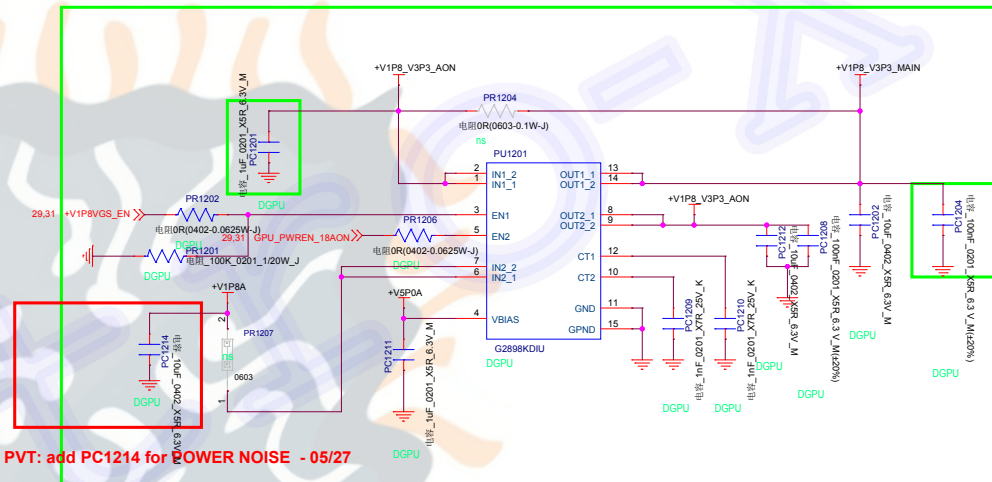
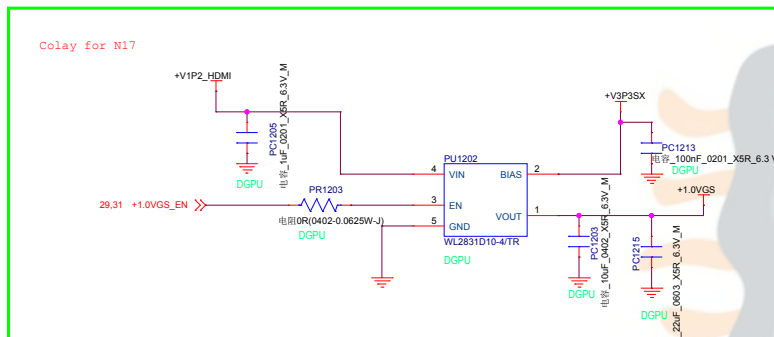
Table 7. Output EDP-Continuous

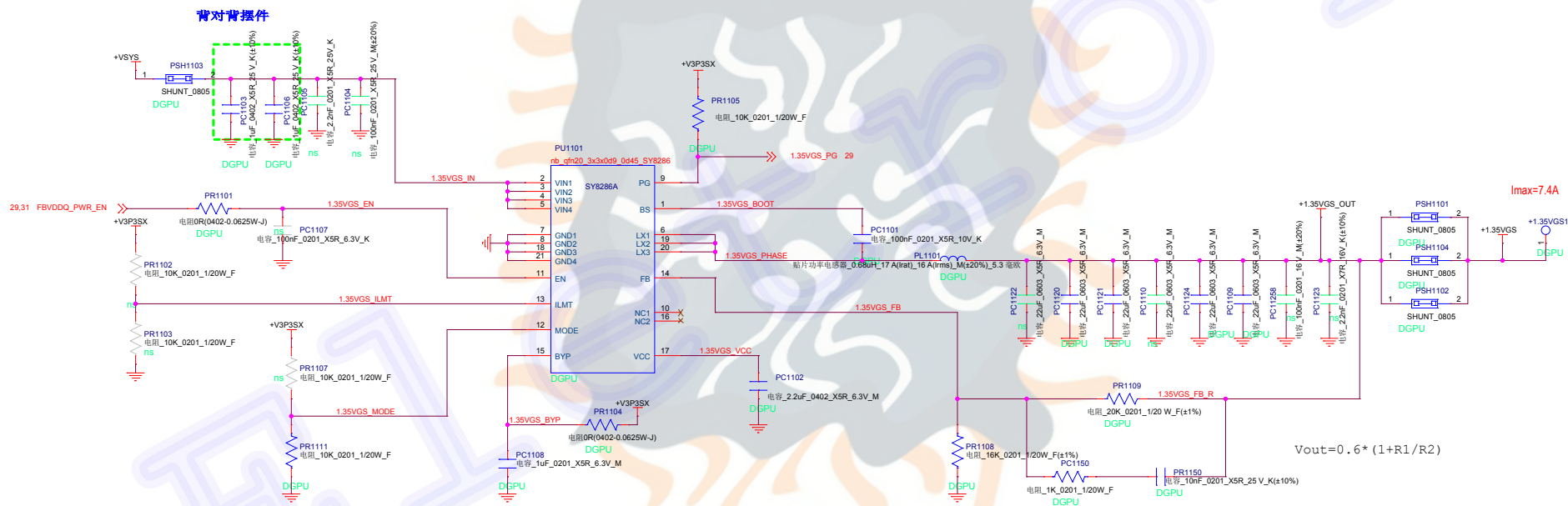
	NVVD	GPU.FBIO	FB.Total ¹	1.0V Total ¹	1.8V Total ²
	—	1.35V ⁴	1.35V ⁴	1.0V ⁴	1.8V ⁴
Product	(A)	(A)	(A)	(A)	(A)
N17S-LG	15.4	2.5	5.0	0.1	0.2
N17S-G1	30.0	3.0	5.6	0.1	0.3
N17S-G0 ⁶	27.8	3.2	5.8	0.2	0.5
N17S-G2 ⁶	28.6	3.2	5.8	0.2	0.5

Table 8. Output EDP-Peak

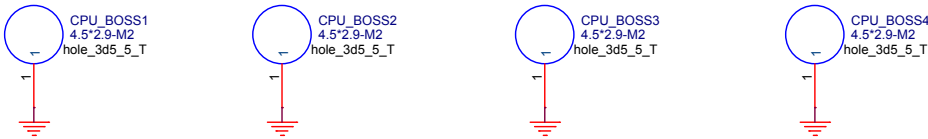
	NVVD	GPU.FBIO	FB.TOTAL ⁴	1.0V Total ¹
	—	1.35V ³	1.35V ³	1.0V ³
Product	(A)	(A)	(A)	(A)
N17S-LG	48.3	2.8	5.8	0.2
N17S-G1	60.1	3.4	6.9	0.2
N17S-G0 ⁶	42.0	3.9	7.4	0.3
N17S-G2 ⁶	60.3	3.9	7.4	0.3







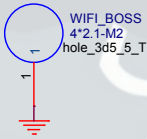
CPU螺母元件 *4



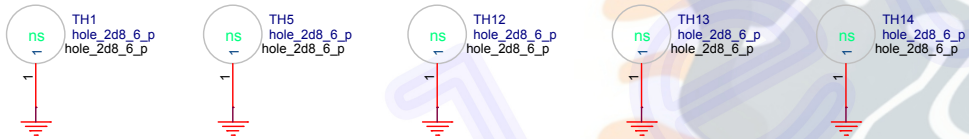
GPU螺母元件 *2



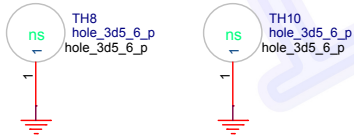
WIFI螺母元件 *1




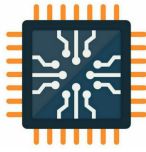
HOLE *5

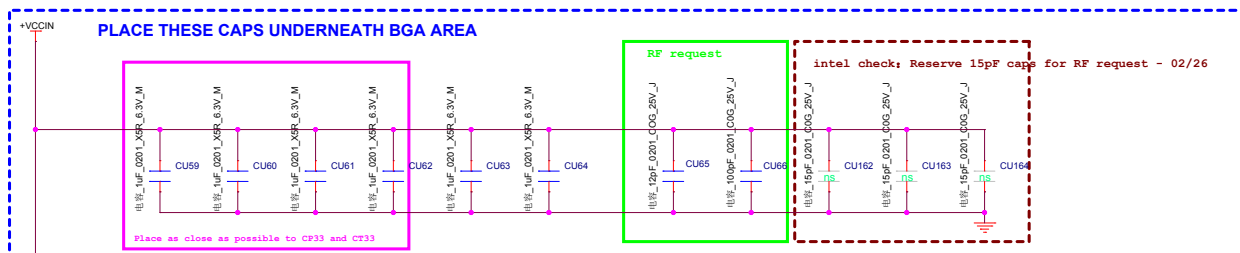


HOLE *2



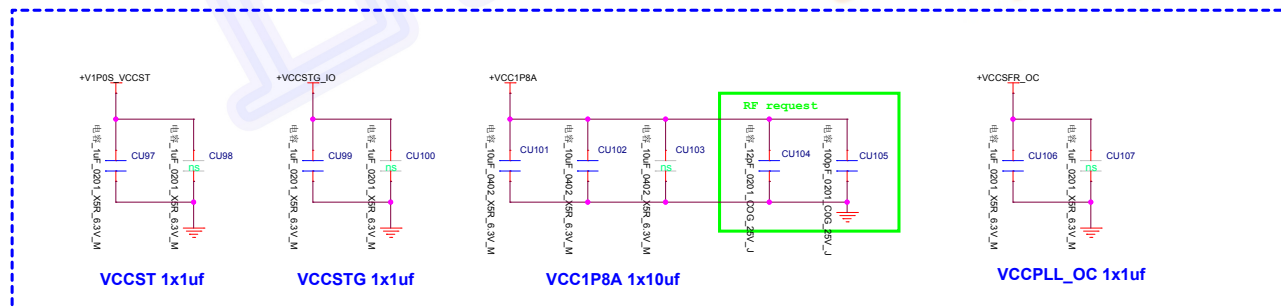
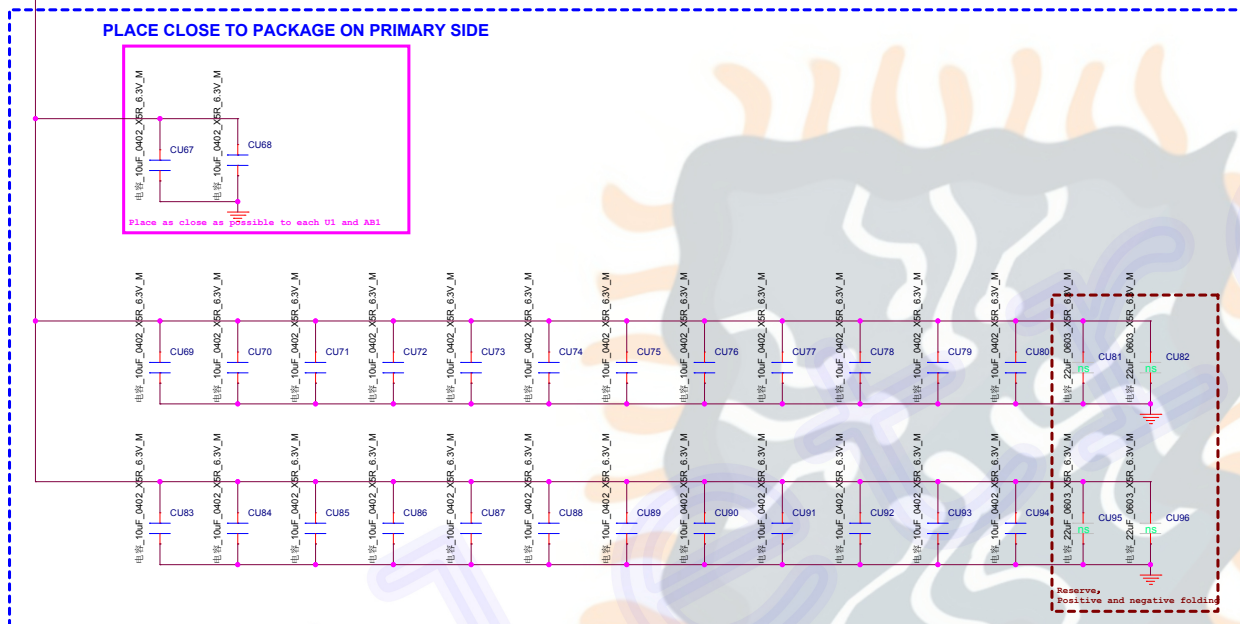
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Date: Monday, July 15, 2019	Sheet: 58	of	72

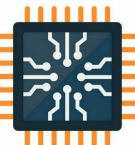
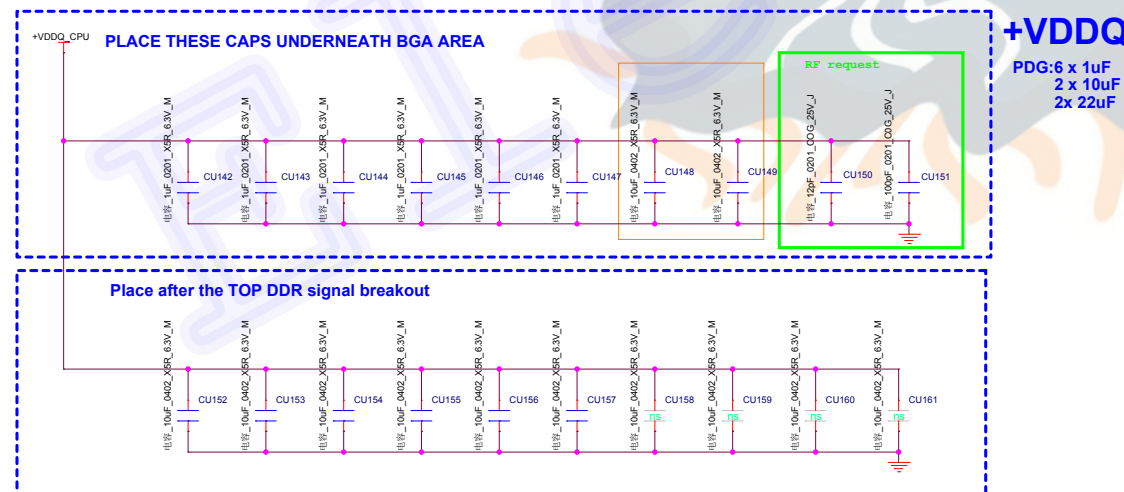
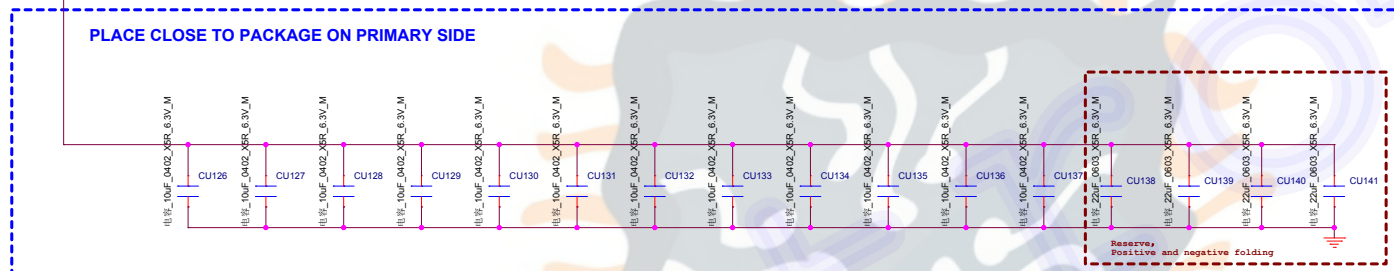
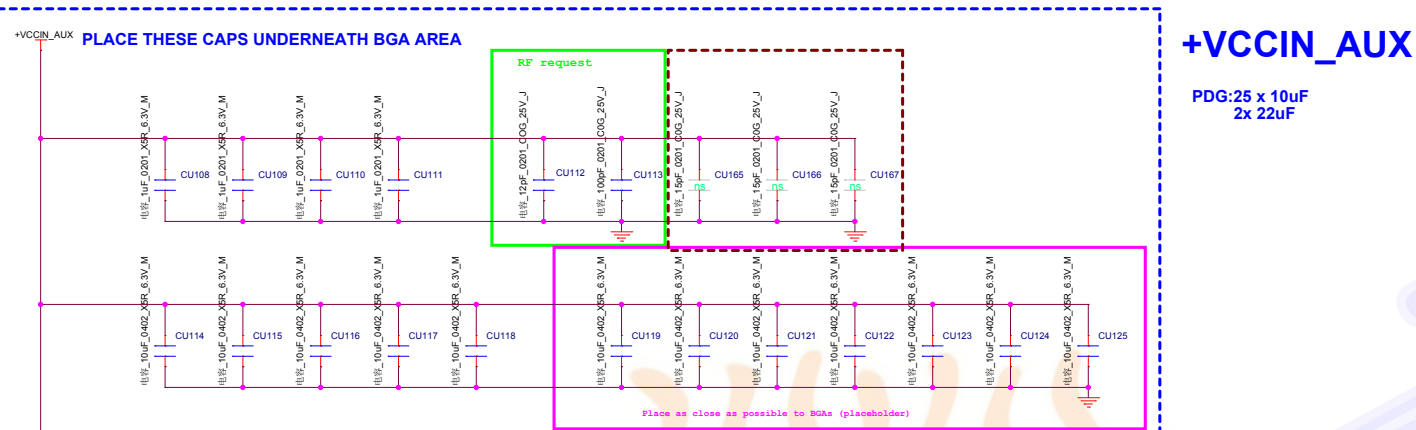




+VCCIN

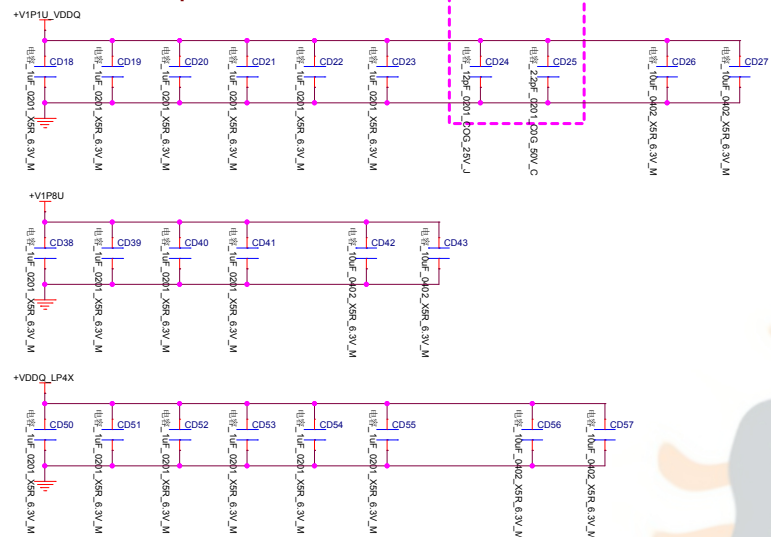
PDG: 4 x 1uF
2 x 10uF
10x 22uF
3x 47uF



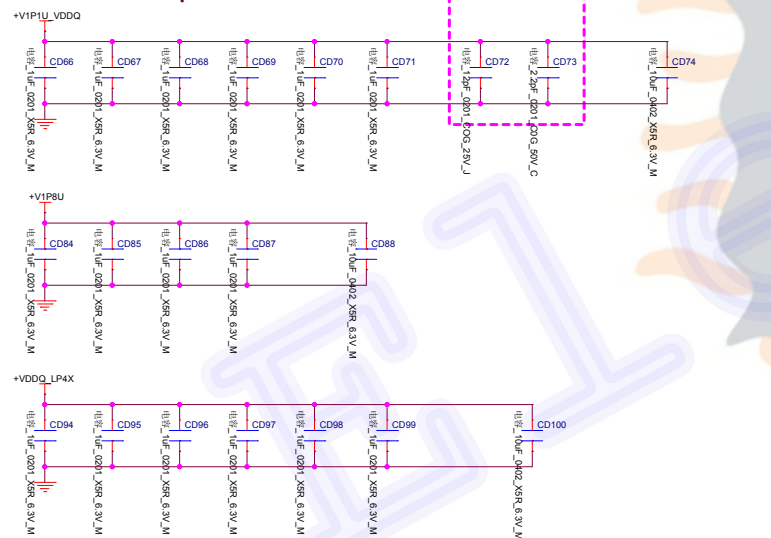


DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL A

Place as close as possible to UD?

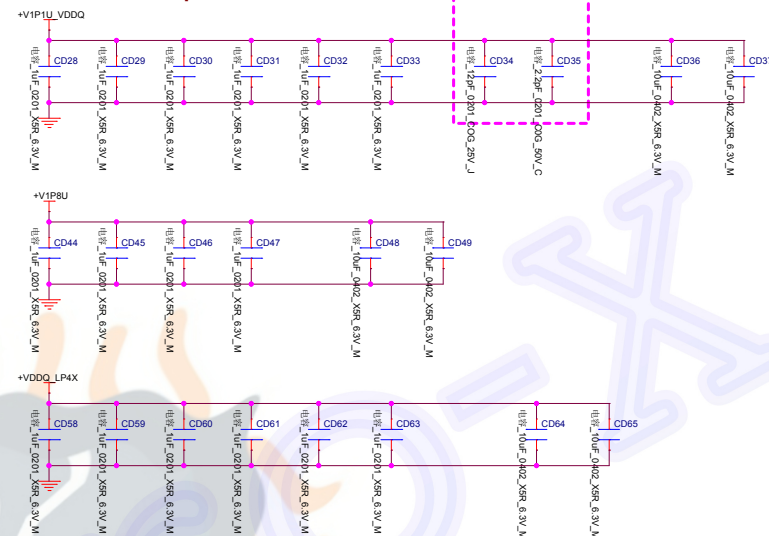


Place as close as possible to UD?

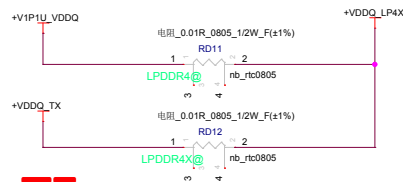
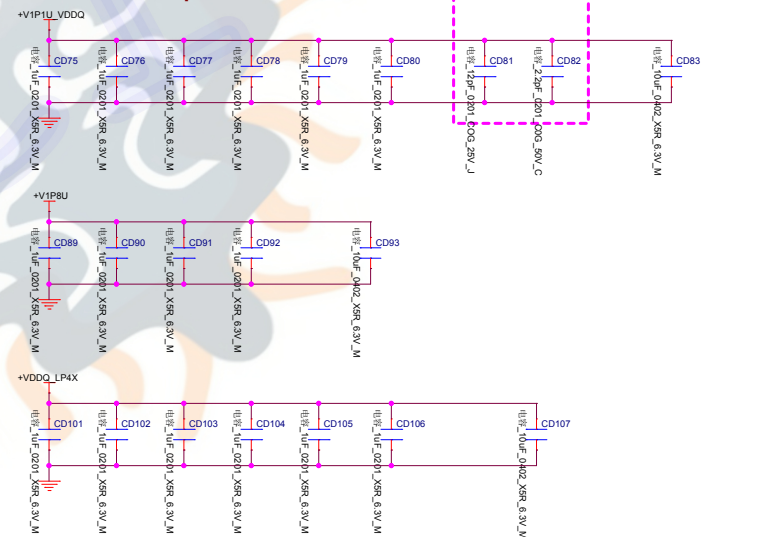


DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL B

Place as close as possible to UD?




Place as close as possible to UD?

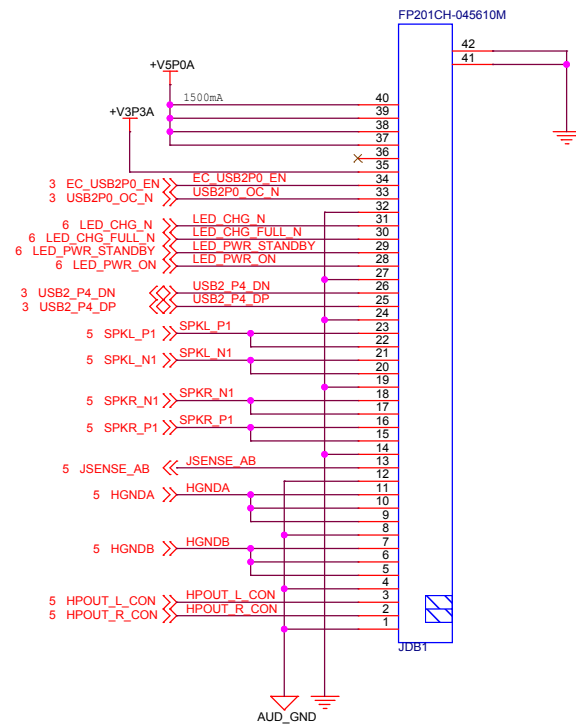


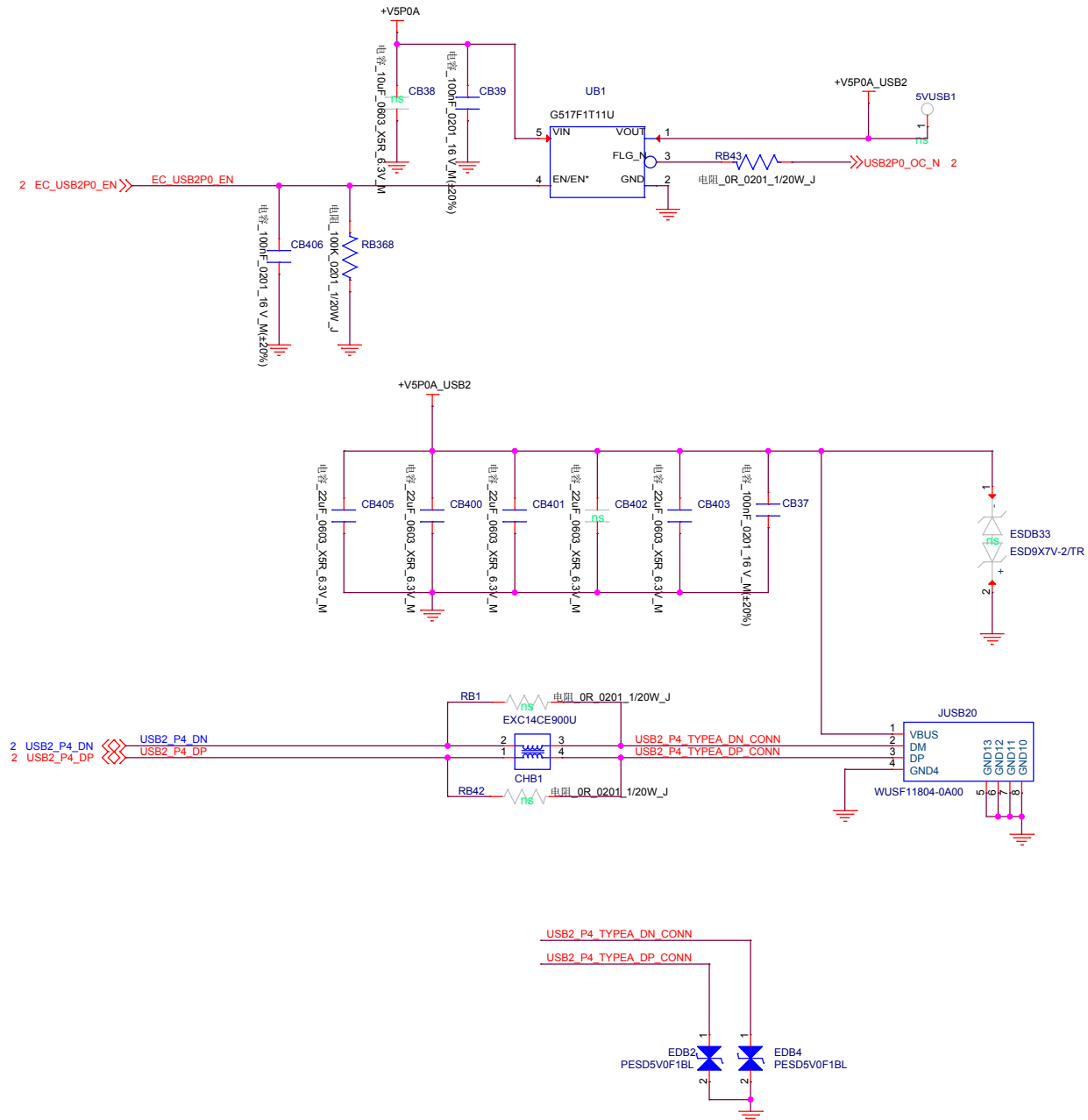
HuaQin Confidential

NB8511 DB Schematics Document

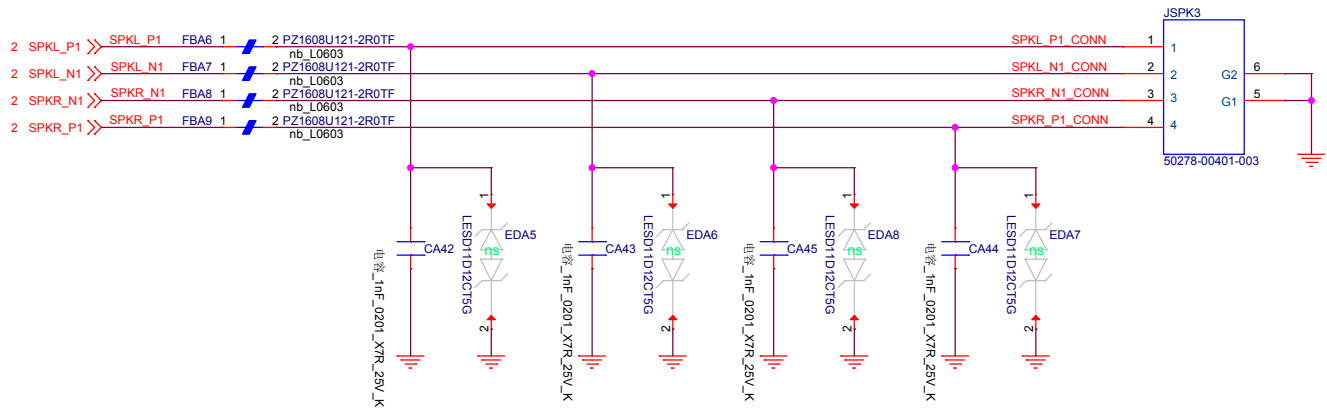
USB BOARD

		Huaqin Telecom Technology Com.,Ltd.	
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Size: A4	Project Name: NB8511		REV: V1.0
Date: Wednesday, July 10, 2019		Sheet: 1	of 10





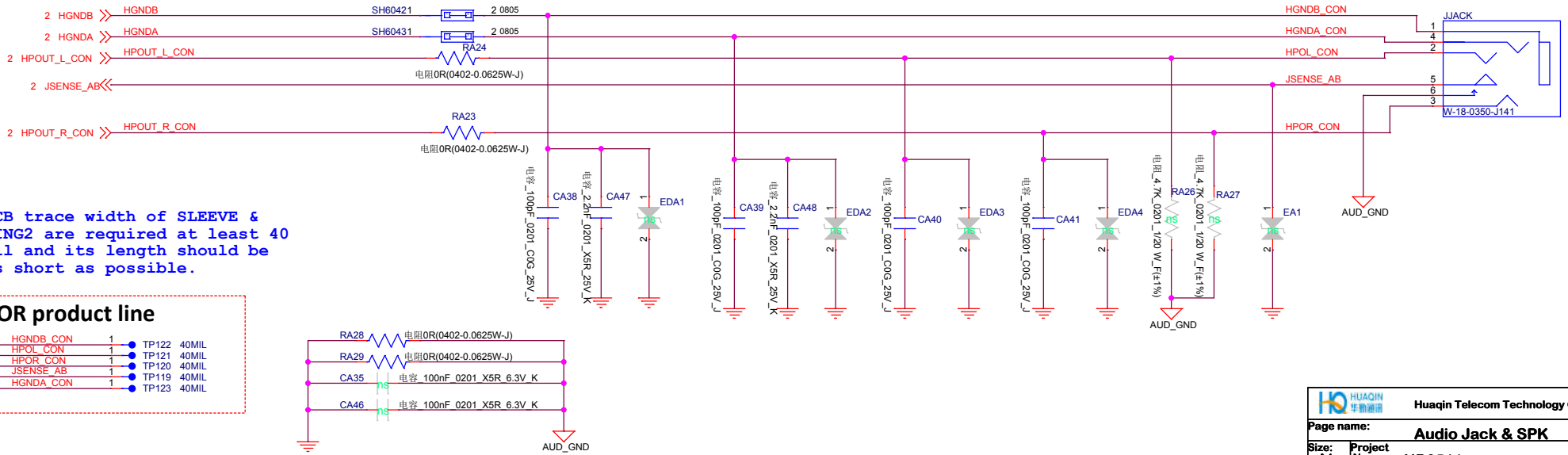
SPEAKER



FOR product line

SPKL_P1_CONN	1	TP127	40MIL
SPKL_N1_CONN	1	TP126	40MIL
SPKR_P1_CONN	1	TP124	40MIL
SPKR_N1_CONN	1	TP128	40MIL

Combo Jack

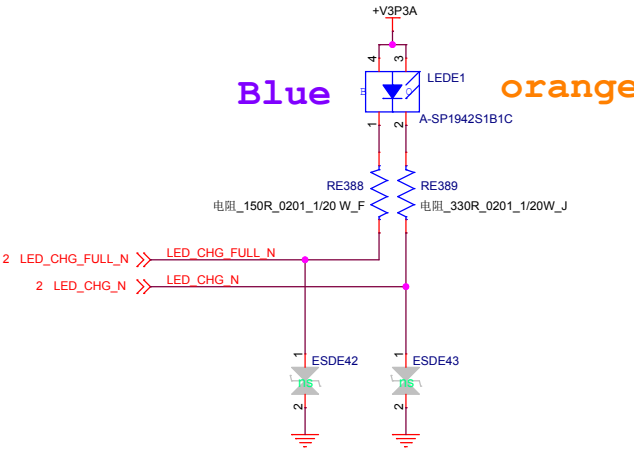
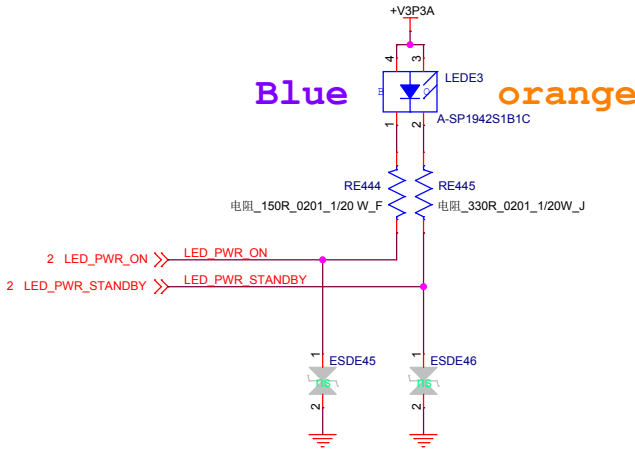


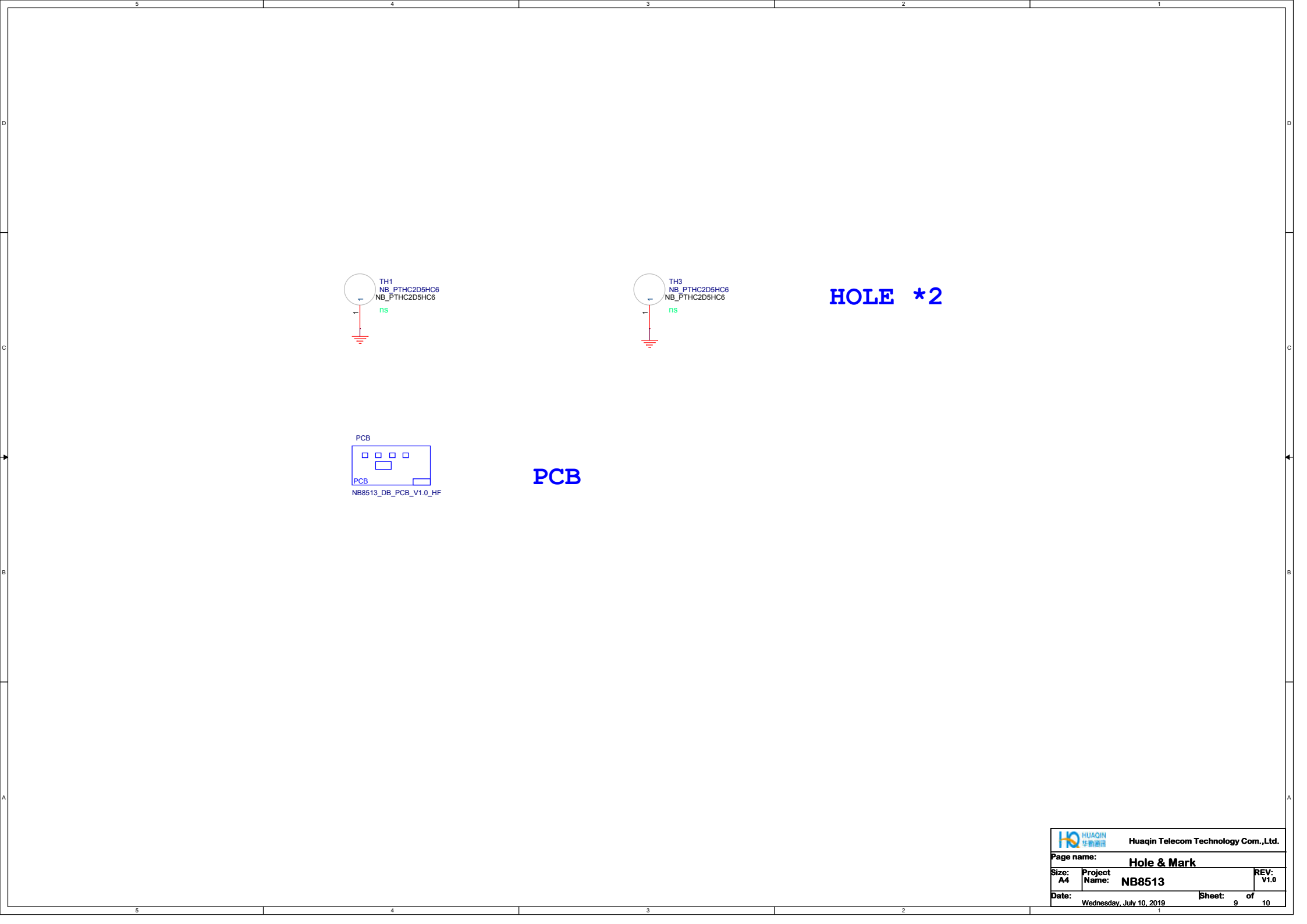
PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.

FOR product line

HGNDB_CON	1	TP122	40MIL
HPOL_CON	1	TP121	40MIL
HPOR_CON	1	TP120	40MIL
JSENSE_AB	1	TP119	40MIL
HGNDA_CON	1	TP123	40MIL

LED





HOLE *2

PCB